
Demo Guide

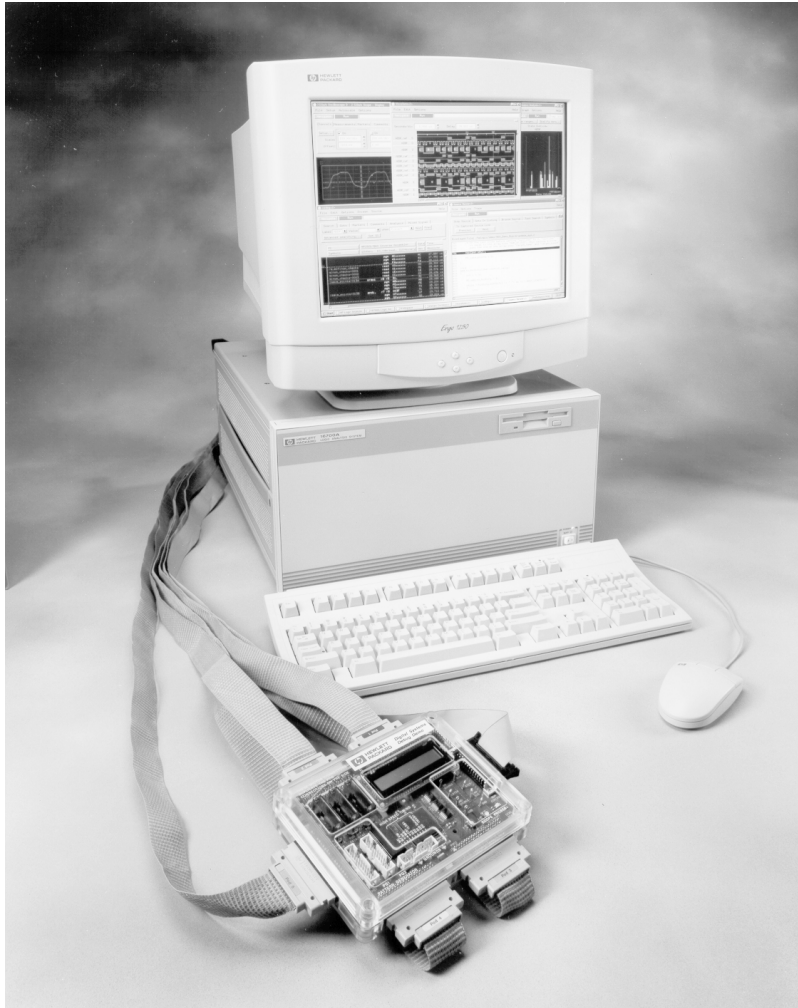
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HP 16700A-Series Logic Analysis System

The HP 16700A-Series Logic Analysis System Reduces Time to Insight



With the HP 16700A-series logic analysis system:

- You can view target system behavior at many different levels of the design hierarchy: from analog signals (using an oscilloscope module), to the timing relationships of signals, to microprocessor execution, to source code, to bus execution, to overall system performance. Being able to look at a problem from many perspectives helps you gain insight into problems faster.
- You can time-correlate different views of target system behavior (and use multiple views) to analyze the same target system event in different ways.
- You can use a pattern generator module to provide stimulus to parts of the target system when testing hypotheses or analyzing the target system's response to specific inputs.
- You can use an emulation module to control microprocessor execution (run, stop, step, breakpoints) and display and modify the contents of microprocessor registers and memory.
- You can explore data collected from your target system, perhaps data that captures a rarely occurring problem, in a more efficient way by taking deep-memory traces and by using post-processing filtering tools. You can also trigger on a specific sequence of events and store only the data of interest to capture execution over a longer time.
- You can export critical data from your target system, import it later, and compare it to new data.
- You can share the networked logic analysis system among project team members to facilitate communication and collaborative debugging.
- You can solve problems quickly and move on to the next problem, speeding up your overall development time.

These capabilities let you identify problems and track them to their root cause. They let you explain all the symptoms of a problem and give you confidence in your solution.

In This Book

This demo guide shows many of the things you can do with the HP 16700A-series logic analysis system. It's part of a demo kit that includes a MPC860 microprocessor-based system.

You can probe the MPC860 demo board by connecting the logic analyzer modules and emulation modules. Later you will connect the oscilloscope, pattern generator, and high-speed logic analysis modules. Then, you can follow the instructions in this guide to capture and analyze MPC860 demo board execution. You will see some of the more powerful ways you can use the logic analysis system to debug and verify your own target systems.

This demo guide shows:

- You can quickly set up the logic analysis system to capture hundreds of waveforms. You can also use the Setup Assistant to quickly trace microprocessor execution, inverse assemble the microprocessor trace, perform run control functions, and correlate source code.
- You can quickly find hardware and software interaction problems by correlating views of the captured data with traces of microprocessor execution, and by analyzing system performance.
- You can quickly find the cause of difficult hardware problems using HP's deep-memory logic analyzers, high-speed logic analyzers, and pattern generators.

This demo guide also contains an appendix that describes the MPC860 demo board and its firmware in more detail and state and timing.

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Getting Started

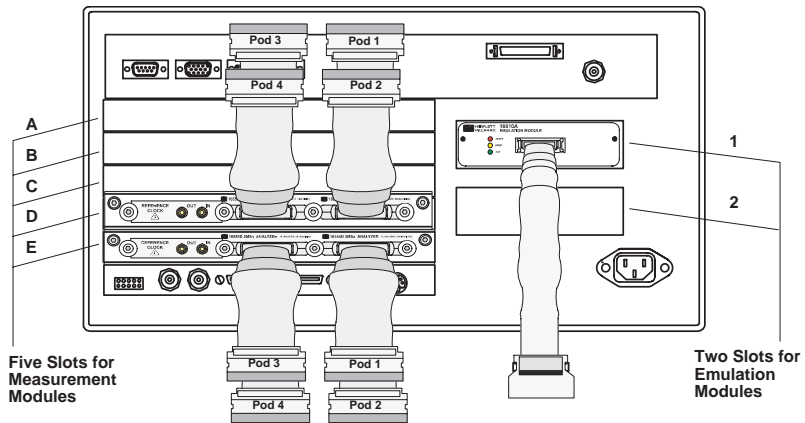
Connecting the demo board to analyzer

The following provides instructions for connecting the demo board to the logic analyzer. The instructions, as well as the entire guide, assume that your analysis system has the recommended configuration of modules.

Go to “Recommended Demo Configuration” on page 151 for instructions on verifying your configuration.

If the logic analysis system does not have the recommended configuration, you can still connect the demo board by following the instructions provided by the Setup Assistant (go to “Using the Setup Assistant” on page 29). However, some of the exercise may not work properly; this will depend on the particular configuration you use.

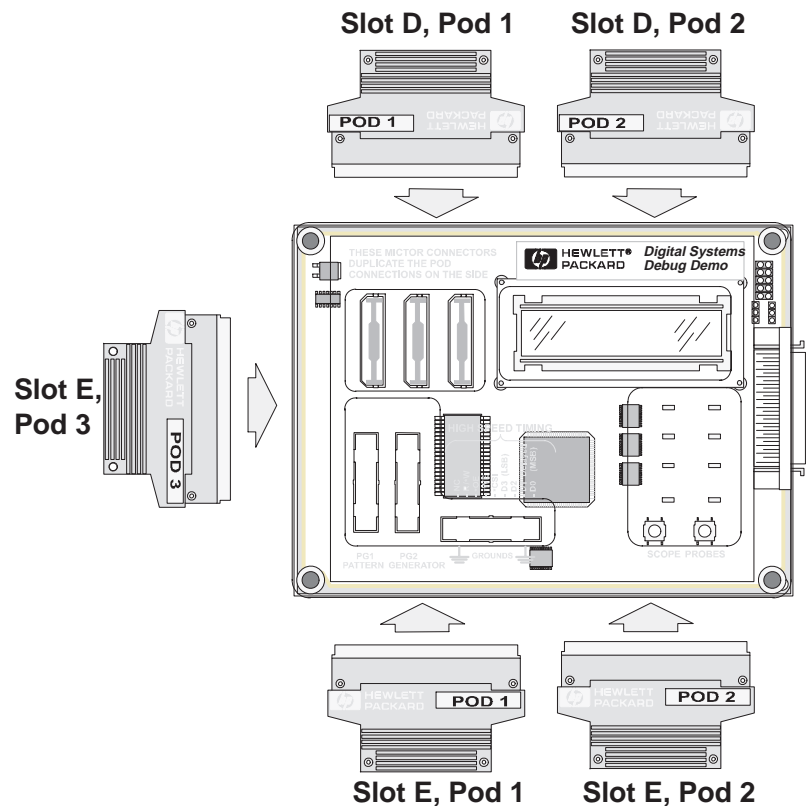
First connect the logic analysis modules. There are two, four pod modules that provide the five pods of logic analysis required for some of the exercises. The analyzers are connected together internally, with the module in slot E serving as master and the module in slot D serving as expansion.



Connecting the first two pods are straight forward, connect pod 1 and 2 of the master analysis module to the 1 and 2 pod locations on the lower edge demo board, away from the LCD

display. The remaining connections are less straight forward and are as follows:

Demo board	Logic Analyzer
Pod 3	Slot D, Pod 1
Pod 4	Slot D, Pod 2
Pod 5	Slot E, Pod 3



As you can see in the picture above, there are two pods 1 and 2. Follow the table carefully to get the right connections. The pods must be connected in the order described above so the

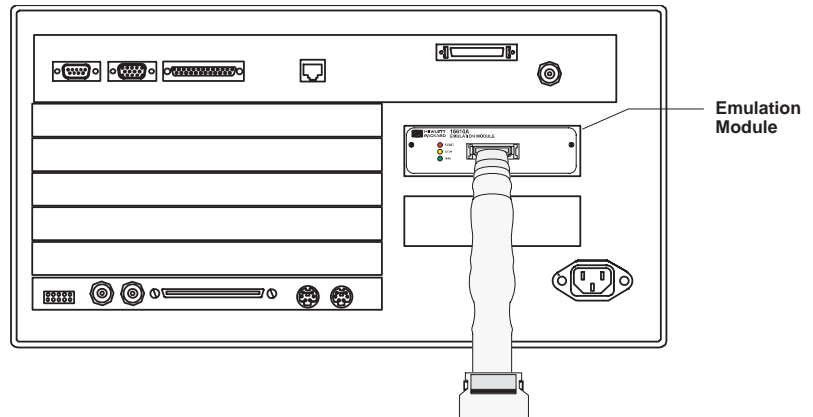
timing measurements, pod 5 on the demo board, can be made on the master analysis module.

NOTE:

Only connect the pattern generator data pods when a particular demo exercise requires them. When the pattern generator data pods are connected, the pattern generator by default takes control of the LCD display. When this happens, the processor will make 2,000 attempts at writing to the display before going on with program execution. Needless to say, this significantly slows down the execution of the demo board code and will affect measurement results.

Connecting the demo board to the emulation module

Now, connect the emulation module.



Notice in the previous picture of the back of the logic analysis system that there are two emulation module slots. This is so that you may control more than one processor at a time.

If the emulation module cable is not connected to the emulation module, do so now. Connect the other end of the cable to the demo board. It goes on the edge with no logic analyzer cables connected to it.

Quickly Set Up the Analysis System

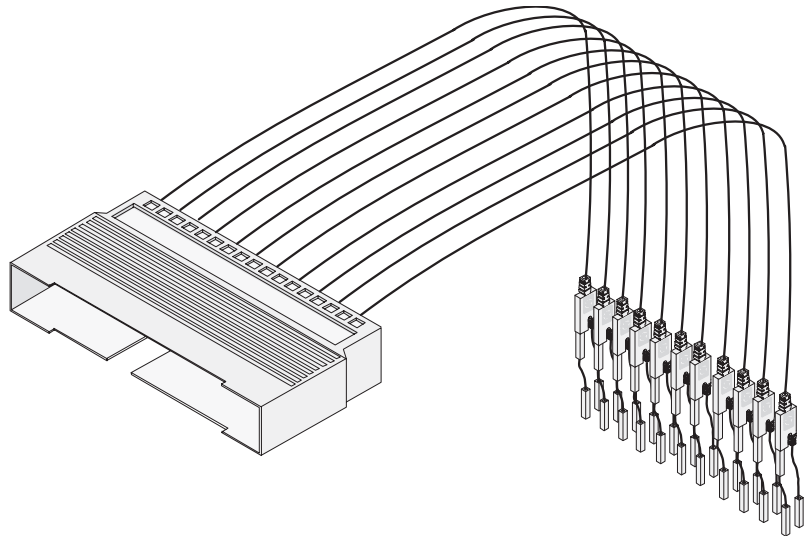
Tracing Hundreds of Your Target's Signals

Being able to capture and display a large number of logic analyzer channels helps you look at more target system execution at one time.

- By using a logic analyzer's flying lead set, you can probe and look at digital signals in any part of a target system.
- By loading the HP 16700A-series logic analysis system with logic analyzer cards and using the logic analysis system's display capabilities, you can easily view and manage a large number of waveforms.

Connecting the analyzer to your target

The most common way to probe a target system is with a flying lead set. The flying lead sets connect to logic analyzer pods to provide 16 individual data connections and one clock connection. HP provides a variety of clips and connections that attach to the flying leads and make it easier to attach to fine-pitch leads.



Two other methods for attaching the analyzer to your target system are discussed at the beginning of the next exercise.

Using an HP logic analysis module

HP has a variety of logic analysis modules for tracing your target system's signals. They range in channel count, trace depth, and acquisition speed. This exercise uses two of the HP 16555D logic analysis modules that have been tied together to function as one analyzer. However, it pretty much applies to all HP analysis modules. For an exercise specific to deep trace, go to "Capturing Very Deep Traces" on page 104.

In this exercise, you will see how the large windows and features of the HP 16700A-series logic analysis system make it easy to manage a large number of waveforms. The HP 16700A-series logic analysis systems can be configured with as many as 1,020 channels of analysis.

1 Probe the MPC860 demo board.

Follow the instructions in the "Getting Started" chapter on page 9 for connecting the logic analysis module to the demo board.

NOTE:

The emulation module connection should NOT be made; it could put the processor into reset, preventing it from running, which is necessary for this exercise.

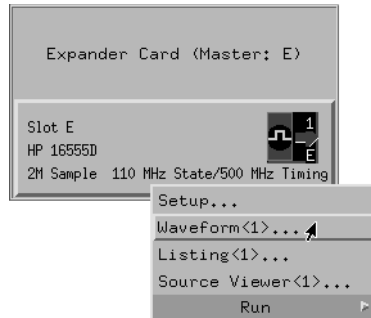
2 Start with the default configuration.

To get a default configuration, go to the "16700A Logic Analysis System" window, select the "Exit" button in the lower right-hand corner, and click "OK" in the dialog that comes up.

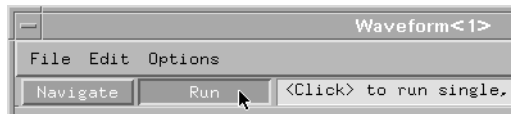
When the session has ended, go to the "Session Manager" window, and select "Start Session on This Display".

3 Set up trigger, and run measurement

When the “16700A Logic Analysis System” window has come up, select the “HP16555D” button on the left-hand side and select “Waveform<1>...” from the popup menu.



Click the green “Run” button to take a trace of the lower 16 bits of the address bus.

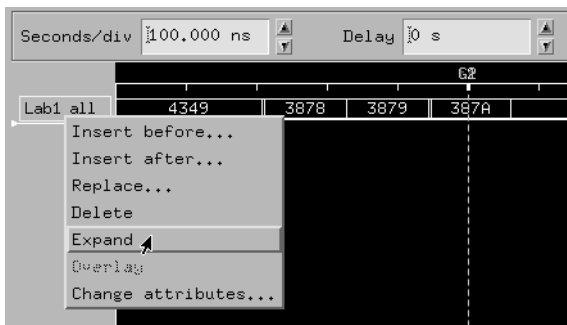


4 Display the captured data.

Maximize the “Waveform<1>” window.

You are looking at an overlaid trace of 16 bits of the address bus; in other words, each of the individual traces of the address bus bits are displayed in this one trace. You can see the hexadecimal value of the address bus where there is space to display it.

To see each individual address line, right-click on “Lab1 all” and select “Expand”. Notice that each “Lab1” is now individually numbered.

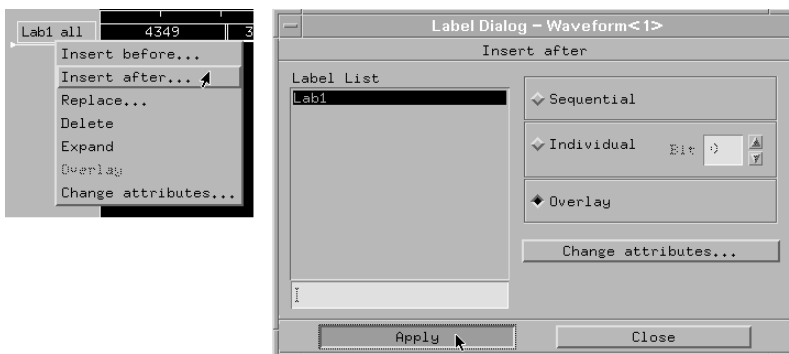


To overlay the lines again, right-click on one of the “Lab1” signals, and select “Overlay”.

5 Replicate the one occurrence of “Lab1 all” several times.

To get to the point of this exercise, managing a large number of waveforms, the Lab1 trace will be replicated multiple times.

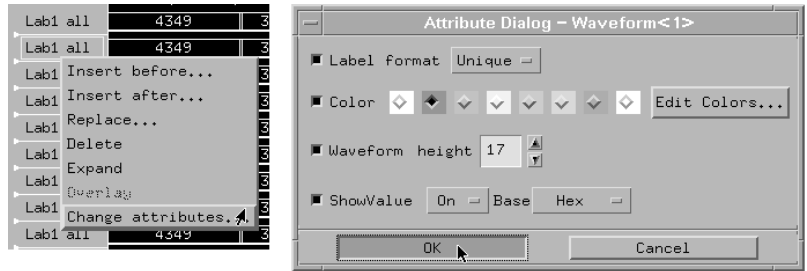
Right-click on “Lab1 all”, select “Insert after...”, and a label dialog comes up. This dialog lets you add more labels to the display, either one bit at a time or as overlaid signal sets. The default is overlaid. Add 9 more of the overlaid “Lab1 all” to the Waveform<1> window by clicking “Apply” 9 times; then, close the dialog.



6 Add color to waveforms.

We now have a total of 160 waveforms displayed. To help identify them more easily, you can add some color.

Pick the second “Lab1 all” from the top, right-click on it, and select “Change attributes...”. Select the red radio button to the right of “Color” and click “OK”.



Try changing some of the other “Lab1 all”.

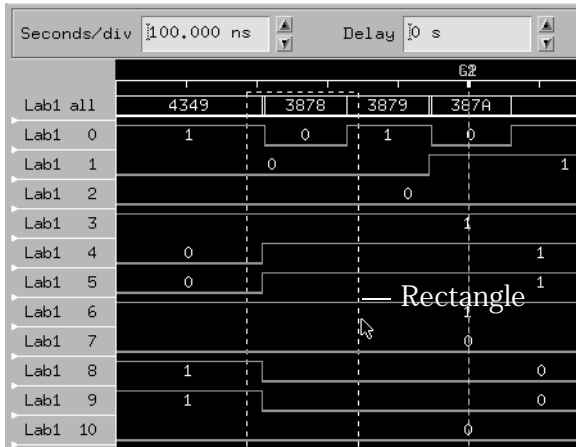
Now, expand one of the colored “Lab1 all” and see how the coloring helps you to follow the timing waveforms.

7 Zoom in on the information of interest.

Pick an area in the waveform trace that you want to look at more closely. Left-click inside the black waveform display area to the left of the area of interest to you. Drag the mouse to the right side of the area you are interested in. This will display a rectangle encompassing the area that the display will be expanded to.

Chapter 2: Quickly Set Up the Analysis System

Tracing Hundreds of Your Target's Signals



When you let go the mouse button, the display will expand horizontally so you can better see the area you are interested in.

- 8 Use timing markers to establish the timing relationship between edges in the waveforms displayed.

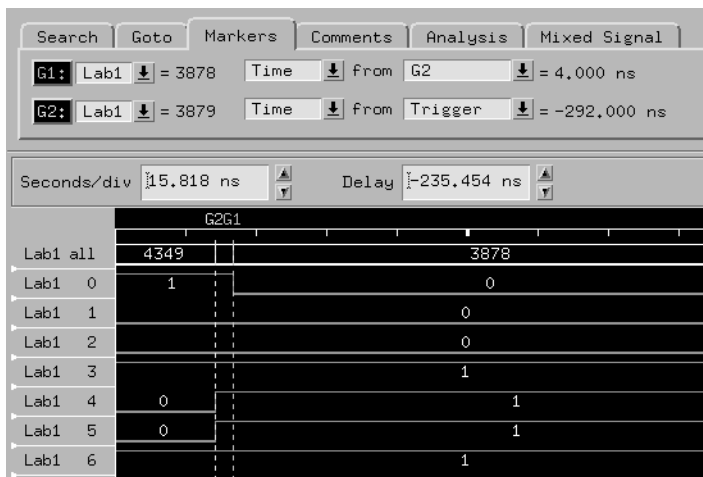
Right-click on an edge that you are interested in, select “Place Marker >”, and select “G1”.



Right-click on another edge that you would like timing information about relative to the G1 marker, and select “G2”.

Select the “Markers” tab and select the list arrow next to the text window for the G1 marker that says “Trigger”.

Select G2 from the list. What you see displayed to the right of the G1 marker line is the time between the G1 and G2 markers.



If you would like to learn more about the analysis system's search capabilities, go to "Capturing Very Deep Traces" on page 104.

Summary

By using the logic analysis system's large display capabilities, you can easily view and manage a large number of waveforms.

Tracing Processor Code Execution with Source Code Correlation

HP's Processor Solutions

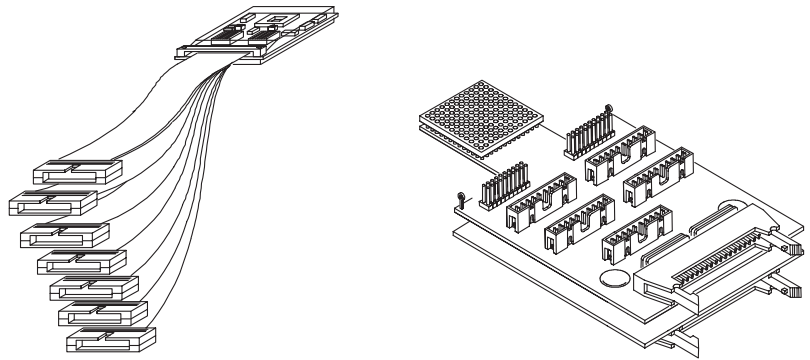
Probing target system circuits can be difficult. The narrow spacing of surface mount package pins and the dozens of connections that a microprocessor requires might make the task seem almost impossible.

However, HP and its channel partners provide products that make probing surface mount packages and microprocessors easier. HP also provides products like emulation modules and the source correlation tool set that make debugging microprocessor execution easier.

Analysis Probes

HP and its channel partners provide *analysis probes* for probing microprocessors and standard buses. Analysis probes are available for over 200 microprocessors and standard buses.

Analysis probes provide the mechanical connection, electrical connection, active circuitry (when necessary), and the software required to trace and inverse assemble microprocessor execution. The following demo, "Using an HP logic analysis module" on page 18, will give you a good feel for the benefits provided by analysis probe software.



Analysis probes plug into Pin Grid Array (PGA) sockets, bus connectors, and even clamp over Thin Quad Flat Pack (TQFP) packages and connect to Ball Grid Array (BGA) footprints. They bring dozens of connections out to logic analyzer pods. Analysis probes are typically low profile compact boards with minimum capacitive loading.

Designing Connections into Your Target System. When probing microprocessor cores embedded in ASICs or when analysis probes cannot be used for some other reason, you can design logic analyzer connections into your target system and purchase an inverse assembler for your processor separately.

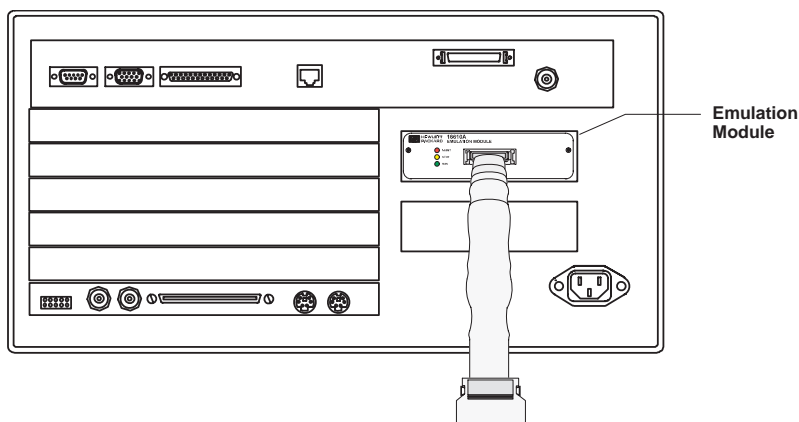
HP provides information on designing several types of logic analyzer connections into target systems (which vary in cost and connection density).

Connectors can range from the 0.1 inch 2x20 connectors (like the five around the edge of the MPC860 demo board) to the high-density Mictor38 connectors (like the three on top of the demo board). The Mictor38 connectors provide connections for two logic analyzer pods each, while the 2x20 connectors provide connections for one logic analyzer pod. The Mictor38 connectors require that you use the HP E5346A high-density termination adapters.

Emulation Modules

The HP 16700A-series logic analysis system can contain *emulation modules* that use a processor's Background Debug Mode (BDM) or JTAG port to control the processor. You can run a microprocessor, stop it, set breakpoints, modify the contents of microprocessor registers and memory locations, and download code to RAM and Flash ROM.

The analysis system can contain up to two emulation modules. This provides support for systems that have both a microprocessor and a DSP, or two microprocessors.



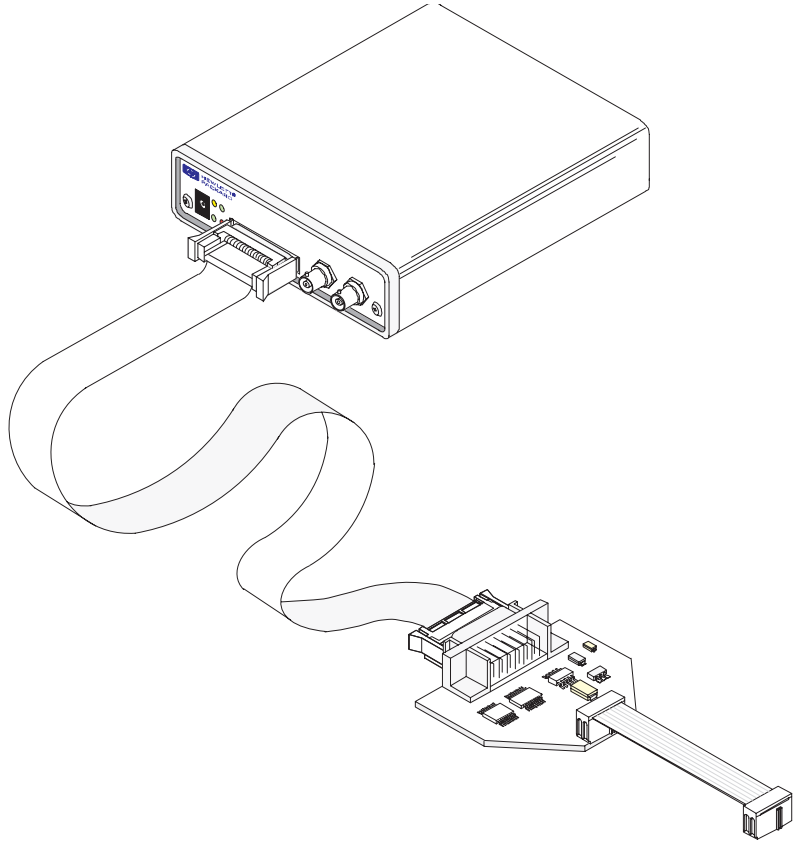
HP's emulation module require a Target Interface Module (TIM) to connect to the processor's BDM or JTAG port (see picture). A different TIM is used for each processor or processor family to adapt the emulation module's connections to the processor's. The 860 demo board that you will be using in the following demo exercises does not need a TIM because we have built it into the board.

Emulation Probes

Emulation probes are just stand-alone emulation modules. They, combined with a commercial debugger, provide an economical run control solution.

Emulation probes can also be accessed from the HP 16700A-series logic analysis system to provide run control for more than two processors.

Below is a drawing of an emulation probe with a TIM attached.



Source Correlation Tool Set

The *source correlation tool set* add-on for the HP 16700A-series logic analysis system lets you view the source code that corresponds to data captured on the microprocessor bus.

The source correlation tool set requires that symbol information be loaded into the logic analyzer from the target system program's object file.

Processor Solution Packages

You can order HP *processor solution packages* that combine an analysis probe, an emulation probe, and the source correlation tool set for a particular microprocessor.

Processor Solution Information on the Web

You can find up-to-date processor solution information on the world-wide web at:

<http://www.hp.com/go/uPsolutions>

Or, contact your HP sales representative.

Using the Setup Assistant

The HP 16700A-series logic analysis system includes a *setup assistant* to help you configure the logic analyzer for a particular analysis probe. It also configures the emulation module for the selected processor and helps you read in your symbol file for the inverse assembly and Source Viewer.

The setup assistant analyzes the configuration of your logic analyzer and the type of microprocessor you want to trace. Then, it asks what options you want implemented. The setup assistant tells you how to connect the analyzer probes, and it creates the necessary configurations.

You only need to run the setup assistant when you start working with a new processor or when you change the configuration of the logic analyzer. Once the setup assistant has created a configuration, it can be saved and reloaded.

The following steps show you how to use the setup assistant to trace microprocessor execution on the MPC860 demo board and view the source code associated with captured data.

1 Start with the default configuration.

To get a default configuration, go to the “16700A Logic Analysis System” window, select the “Exit” button in the lower right-hand corner, and click “OK” in the dialog that comes up.

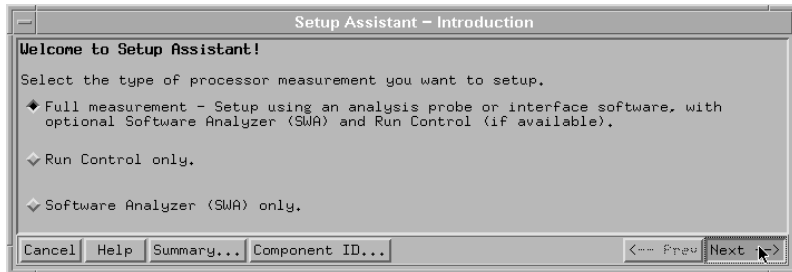
When the session has ended, go to the “Session Manager” window, and select “Start Session on This Display”.

2 Start the setup assistant.

Go to the “16700 Logic Analysis System” dialog and select “Setup Assistant” from the bottom buttons.



The “Setup Assistant – Introduction” dialog will be launched. Select “Full measurement - ...” and then select “Next -->” to go to the next dialog.



3 Identify your microprocessor

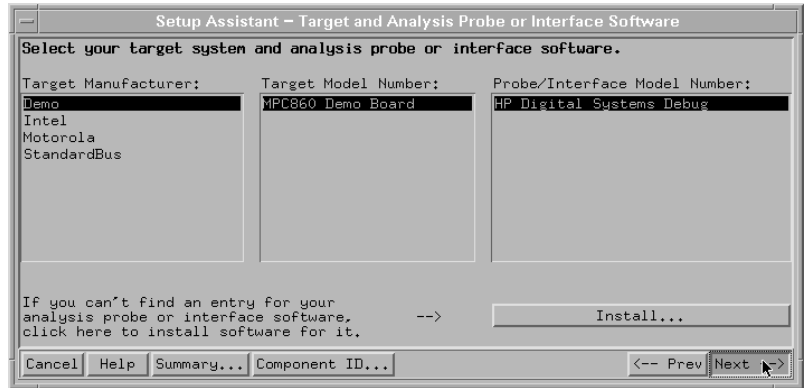
The “Setup Assistant – Target and Analysis Probe or Interface Software” dialog now comes up. This is where you tell the setup assistant what processor you are using and whether you are using an analysis probe or connecting directly to your target.

Microprocessor Support

Processors are added on a regular basis, so if you do not see the one you need, check with your HP sales representative to see if it has become available.

Tell the setup assistant you are using the MPC860 demo board (which has built-in connections for the logic analyzer).

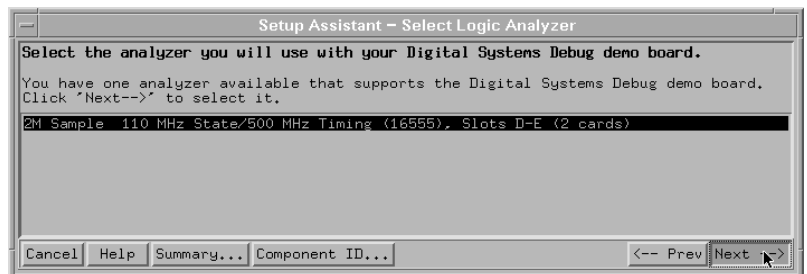
Select “Demo” from the list which expands to “MPC860 Demo Board” and “HP Digital Systems Debug”, then go to the next dialog.



4 Select the logic analyzer.

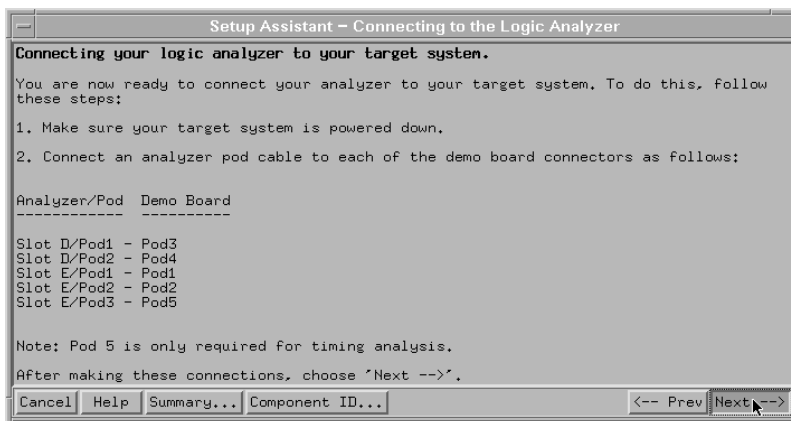
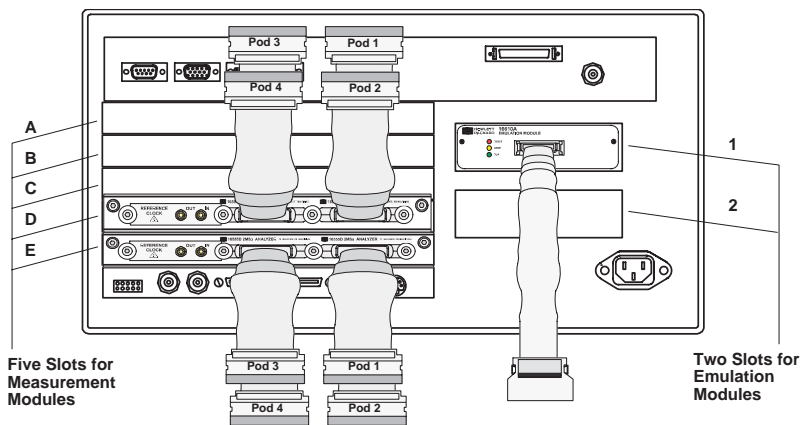
The “Setup Assistant – Select Logic Analyzer” dialog is now up. This dialog presents you with a list of analyzer modules installed in your system that are suitable for the analysis probe you are using.

If you have the standard demo set of modules in your system, only one analyzer is listed. Select the logic analyzer, and go to the next dialog.



5 Connect the demo board to the logic analyzer.

This brings up the “Setup Assistant – Connecting to the Logic Analyzer” dialog. This dialog tells you how to connect the analyzer module to the demo board.



When you are done connecting the logic analyzer to the demo board, select “Next -->”.

The setup assistant now loads the proper configuration for the demo board, and the proper inverse assembler, into the HP 16555D analysis module. Click “OK” to clear the

informational dialogs that pop up during this part of the exercise.

NOTE: Don't connect the pattern generator just yet. The default pattern generator signal level outputs will turn off the MPC860 demo board's LCD display.

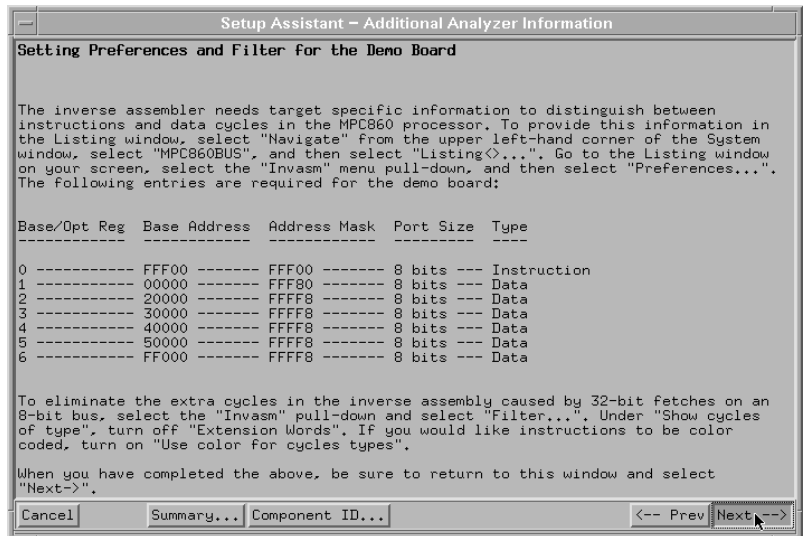
6 Set the inverse assembler preferences and filter for the demo board.

NOTE: It is important that you follow the instructions in the "Setup Assistant - Additional Analyzer Information" dialog. This is not optional.

Follow the instructions in the "Setup Assistant - Additional Analyzer Information" dialog for entering the demo board memory map and for setting up the filter.

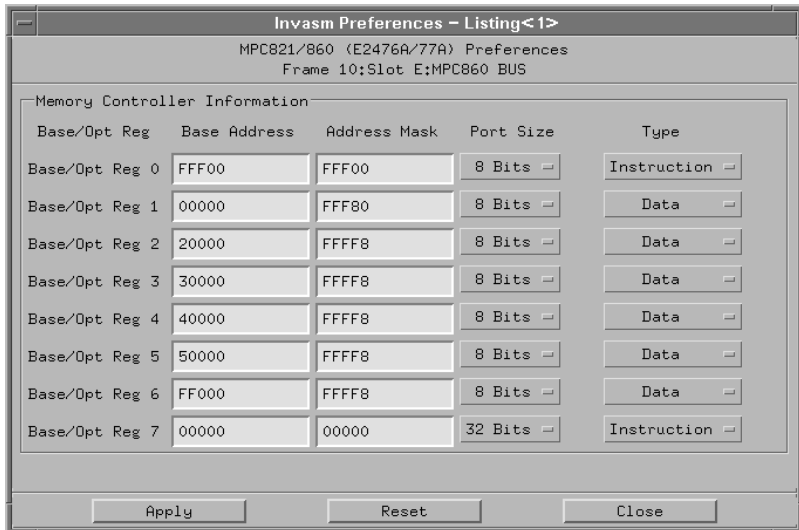
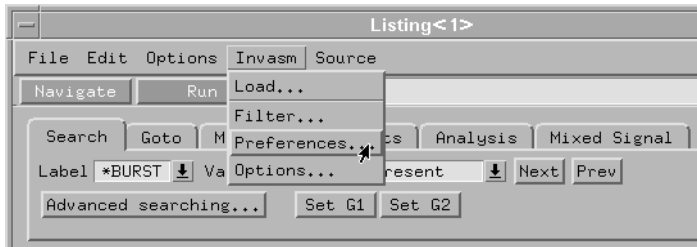
Note that the MPC860 processor does not provide status information that distinguishes between data and instruction fetches. Therefore, you must provide that information.

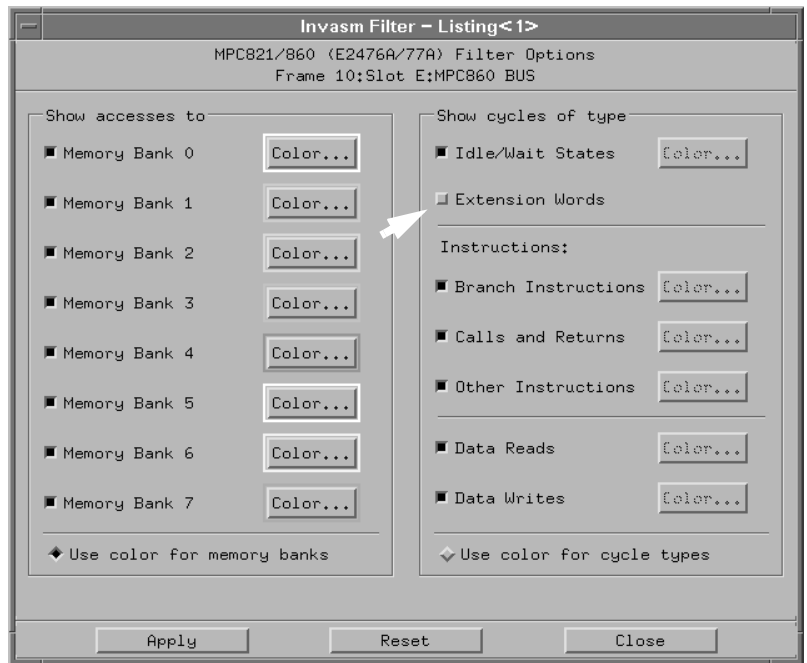
After you have set the inverse assembler preferences and filter for the demo board, go to the next dialog.



Chapter 2: Quickly Set Up the Analysis System

Tracing Processor Code Execution with Source Code Correlation



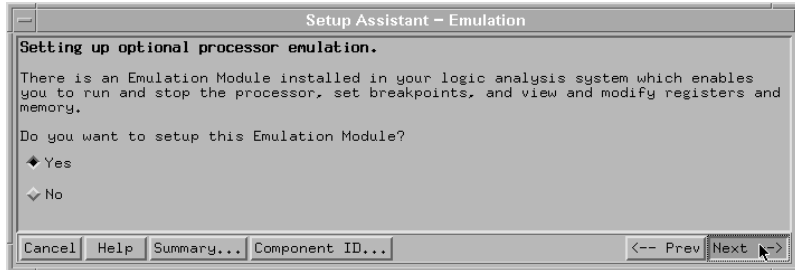


7 Connect the demo board to the emulation module.

The “Setup Assistant – Emulation” dialog comes up at this point.

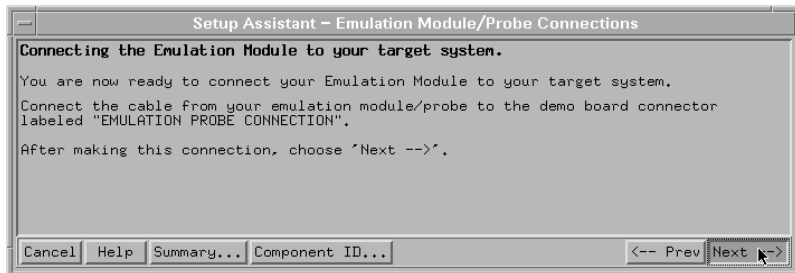
If you have the standard demo set of modules, the setup assistant will detect an emulation module in your system.

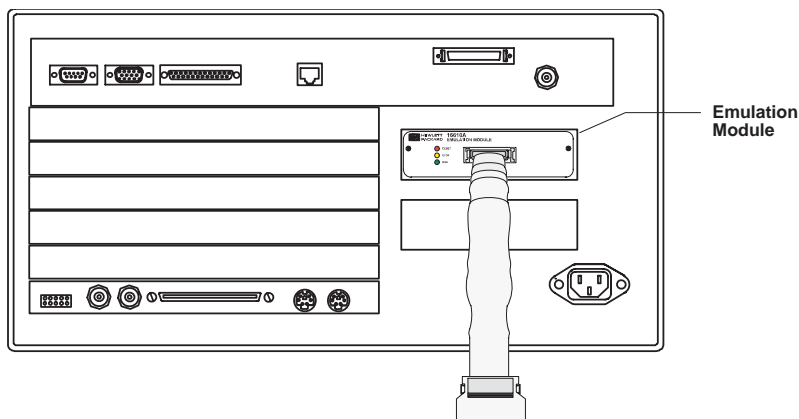
Select “Yes” to have the MPC860 personality loaded into the module, then go the next dialog.



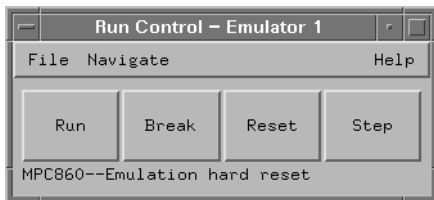
The “Setup Assistant – Emulation Module/Probe Connections” dialog gives you instructions on how to connect the emulation module to the demo board.

When you finish connecting the emulation module cable, proceed to the next dialog.





The setup assistant will now install the MPC860 personality and launch the “Run Control – Emulator 1” dialog.



It is possible to have two emulation modules installed in the system. The second emulation module can be used when debugging dual processor target systems or target systems with digital signal processors (DSPs).

8 Turn on the Source Viewer.

The “Setup Assistant – Source Correlation” dialog should now be up. If it isn’t, it could be that the source correlation tool set license has not been turned on for the system you are using. Contact your HP representative to get this corrected.

Select “Yes” to have the setup assistant install the source correlation tool set. The source correlation tool set lets you

view the high-level source code associated with data captured by the logic analyzer.

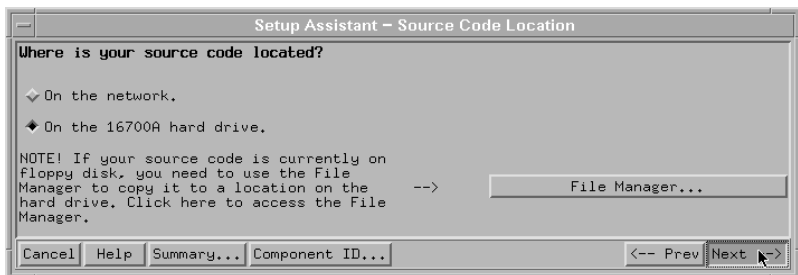


Go to the next dialog.

9 Identify the location of the demo board's source code.

The “Setup Assistant – Source Code Location” dialog helps you load your source code. Source code can be located on a remote computer in your network (if the logic analyzer has been connected to the network), or you could have transferred the source code to the logic analyzer's hard disk. In this example, the source code for the demo board is located on the logic analyzer's hard disk.

Select “on the 16700A hard disk” and go to the next dialog, “Setup Assistant – Symbol Loading”.



10 Load the symbol file.

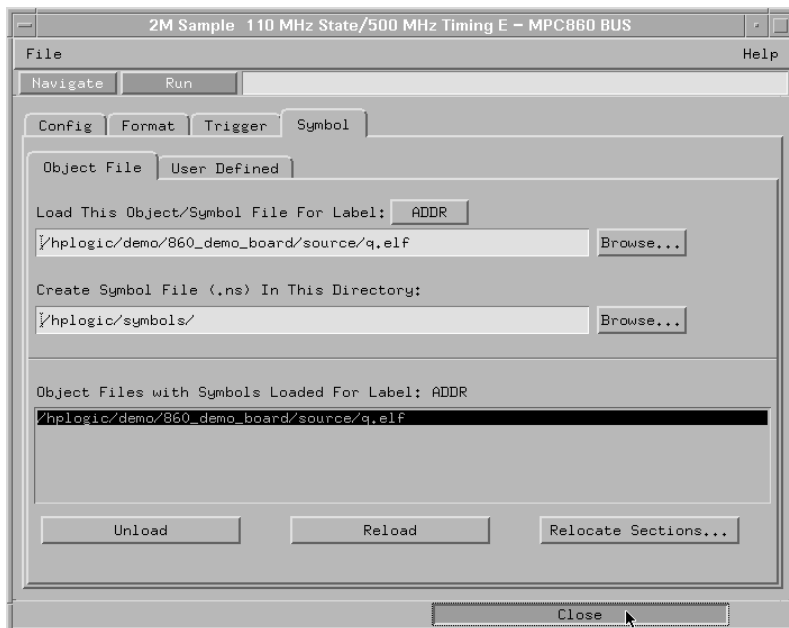
Select “Load Symbol File..”.



The dialog launched is the analysis module’s Setup dialog. The “Symbol” tab has been pre-selected for you. Select the “Browse..” button next to the “Load This Object/Symbol File for Label: ADDR” text box.

Open the demo folder by clicking on the plus symbol in front of it. Open the 860_demo_board folder, select the Source folder, and then scroll down to the file called q.elf.

Select the “q.elf” file in the “demo/860_demo_board/Source” directory, and click the “Load” button. The symbol file for the demo board has now been loaded.



Minimize the “2M Sample 110 MHz State/500 MHz Timing E – MPC860 BUS” dialog.

Go to the next Setup Assistant dialog. You will find that this opens the Source Viewer display and the Listing display. These are the dialogs that you will use to trace the MPC860 microprocessor.

11 Save the configuration.

The “Setup Assistant – Saving to Disk” dialog is now up. This dialog prompts you to save your configuration to disk. If you save the configuration, you can load it the next time you turn

on the analyzer; this lets you configure the logic analysis system without having re-run the setup assistant.



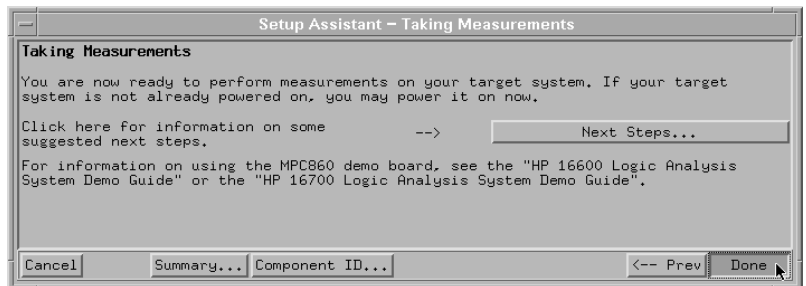
12 Exit the Setup Assistant.

The "Setup Assistant - Taking Measurements" dialog is your last dialog in the Setup Assistant.

What to Do Next

You can get some suggestions about what to do next by selecting "Next Steps". This will take you into the on-line help system.

Since you will be getting help from this demo guide as to what to do next, just select "Done" for now.



13 Start MPC860 demo board execution.

Now you are ready to take a trace. First, you must get the MPC860 microprocessor running. Run Control starts up in reset by default. Click the “Run” button in the “Run Control – Emulator 1” dialog, you should see “MPC860—Running user program” at the bottom of the dialog.

14 Capture MPC860 demo board execution.

Now, click the green Run button in any window and the analyzer will take a trace for you.

15 Display the captured data.

Open the “Listing” display. Scroll through the listing and watch how the source viewer follows along.

Go to the Source Viewer display, select the “Step Source” tab, and click “Previous” and “Next” to step through the source code. Watch how the “Listing” trace follows the source code.

Summary

You can quickly set up the logic analysis system to capture a specific microprocessor’s execution using HP’s probing, run control, source code viewing, and setup assistant tools.

**Quickly Find the Cause of
Difficult HW/SW Interaction
Problems**

Looking at Correlated Hardware/Software Traces

Being able to look at a problem from different perspectives helps you gain insight into problems faster.

- By looking at different areas in a target system and by time correlating the captured data, you can view the flow of data from one part of the target system to the next.
- By looking at the analog values of a signal as well as the digital values and by time-correlating the captured data to a trace of the processor, you can see how hardware symptoms might be caused by a software problem or how software symptoms might be caused by a hardware problem.

Correlating processor execution with external buses

You can follow the flow of data in a target system by capturing and correlating data from different parts of the target system. For example, you can see how data flows from a microprocessor bus to an external bus or port.

Analysis Probes for Standard Buses

Analysis Probes are available for over a dozen buses. This includes PCI, ISA, PCMCIA, SCSI 1, 2, and 3, USB, VME, and more. Analysis probes make it easy to connect the logic analyzer to a bus. They provide circuitry to decode the bus's various states, and they configure the analyzer to correctly present the bus's states in symbolic form.

Visit the HP web site at www.hp.com/go/uPTools, or contact your HP sales representative, for a current list of buses supported by analysis probes.

On the MPC860 demo board, you can capture code executed on the microprocessor bus and correlate it to the waveform trace captured on the asynchronous, serial Controller Area Network (CAN) bus.

Also, you can use the logic analysis system's serial analysis tool set to interpret the waveform trace of the CAN bus.

As is the case in this demo, you can configure a logic analysis module into two "virtual" logic analyzers:

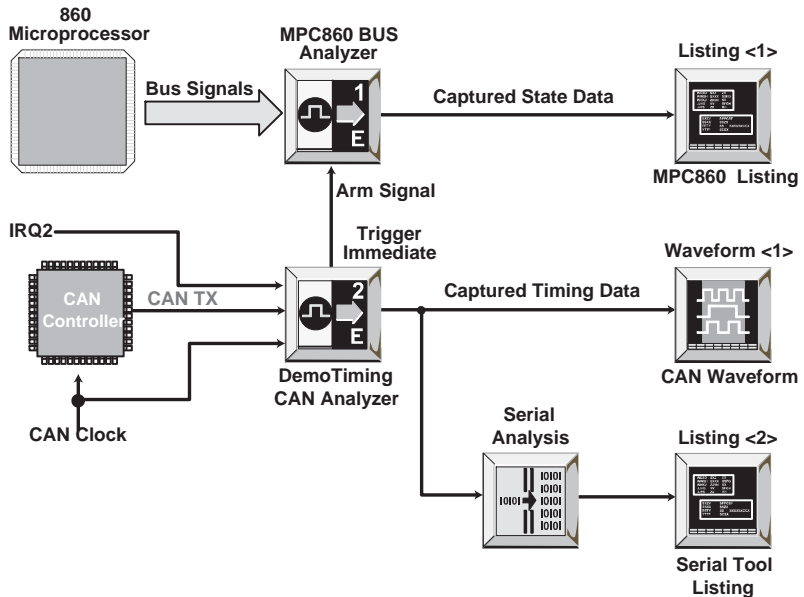
- one logic analyzer that captures microprocessor execution synchronously with the microprocessor's clock (a *state analyzer*).
- one logic analyzer that captures data on the CAN bus asynchronously at sample rate determined by an internal clock (a *timing analyzer*).

(For more explanation of the difference between timing and state analyzers, see “Timing Analysis vs. State Analysis in Logic Analyzers” on page 154.)

The two virtual analyzers can run independently, or, as in this demo, the trigger of the MPC860 BUS analyzer can arm the DemoTiming analyzer.

For this exercise, Analyzer1, called “MPC860 BUS”, is configured as a state analyzer to trace the demo board’s processor. Pods 1 and 2 of the slot E analysis module and Pods 1 and 2 of the slot D module have been assigned to this analyzer. These pods are connected to the processor.

Analyzer2, called “DemoTiming”, is configured as a timing analyzer. Pods 3 and 4 of the slot E analysis module have been assigned to this analyzer. Pod 3 is connected to the CAN bus TX line, IRQ2, and CAN clock.



1 Probe the MPC860 demo board.

Follow the instructions in the “Getting Started” chapter on page 9 for connecting the logic analysis module to the demo board.

NOTE:

Make sure the pattern generator data pods are not connected to the demo board; otherwise, the changes in demo program execution will affect the results of the measurements that follow.

2 Load the configuration files for this demo.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the CAN_bus.____ configuration file from the /hplogic/demo/860_demo_board/configs/hp1670x directory, and click the Load... button.

In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

3 Make sure the MPC860 demo board processor is running in a known state.

Click the “Reset”, “Break”, and “Run” buttons in order.



Resetting the processor starts it from a known state. Breaking puts the processor into the background monitor and allows the emulation module to read the microprocessor's configuration registers (whose contents enable breakpoints among other things).

4 Set up to trigger on a source line.

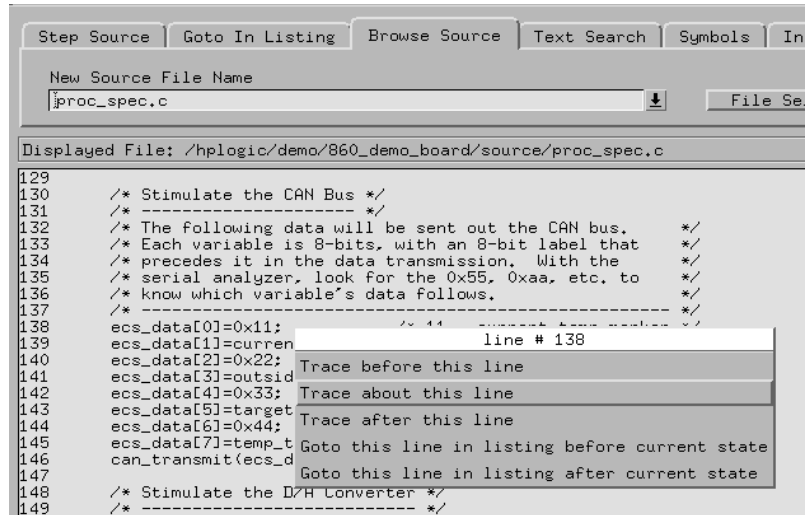
To follow the flow of data from when it is fetched from memory to when it flows on the CAN bus, first trigger the analyzer that captures microprocessor execution when data is fetched from memory.

To set this trigger up, go to the "Browse Source" tab of the "Source Viewer<1>" window, click "File Selection...", select the `/hplogic/demo/860_demo_board/source/proc_spec.c` file, and click OK. This is the source code for one of the main functions executed by the MPC860 demo board.

Scroll down to line 130, which is the beginning of the CAN bus stimulus routine. You can see that this is where the data string that is going to be put onto the CAN bus gets built up. This data string includes marker bytes 11, 22, 33, 44, and temperature bytes.

If you would like to better understand the purpose of the temperature values, see the overview of the code that is executing in the demo board located in the Appendix , "About the MPC860 Demo Board," on page 129.

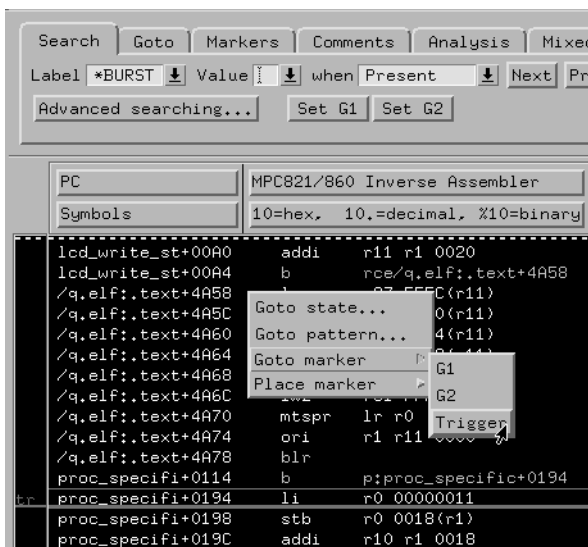
To set up the logic analyzer trigger, click on line 138 and select the “Trace about this line” option. Make sure the heading of the option list says “line # 138”.



- 5 Click the green Run button to perform the measurement.
- 6 Display the captured microprocessor data.

Go to the microprocessor trace listing, right click in the listing area, select “Goto Marker >”, and select “Trigger”. This places the center of the listing on the trigger point. You see that the highlighted line of the source viewer is line 138.

Chapter 3: Quickly Find the Cause of Difficult HW/SW Interaction Problems Looking at Correlated Hardware/Software Traces



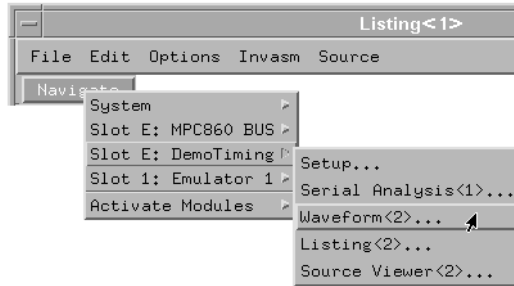
Scroll down through the listing and you see the value of the four temperatures being fetched from memory. The data reads are in yellow. Notice the correct symbols for the temperatures are used in the PC column.

Continue to scroll down until you see the turquoise data writes to the CAN bus controller. You see that the temperature markers and then the temperatures were written to the controller. You then see that a 0x43 and 0xE6 was written to the controller. This told the controller to transmit the data.

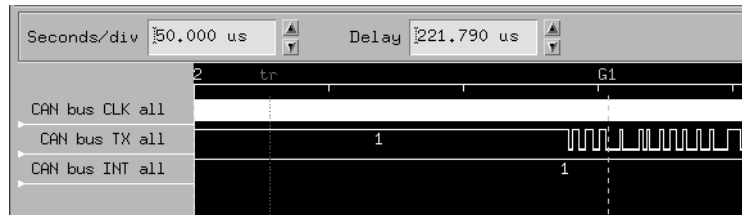
7 Display the captured CAN bus data using the serial analysis tool set.

Now, verify that the correct data was transmitted on the CAN bus.

Click one of the “Navigate” buttons. Select “DemoTiming >”, and select Waveform<2>.



This brings up the waveform trace of the CAN bus that was taken when you last ran the analyzer. It is a trace of the CAN clock, CAN transmit line, and CAN interrupt line. The trigger point on the trace is the same trigger point that is on the processor listing.



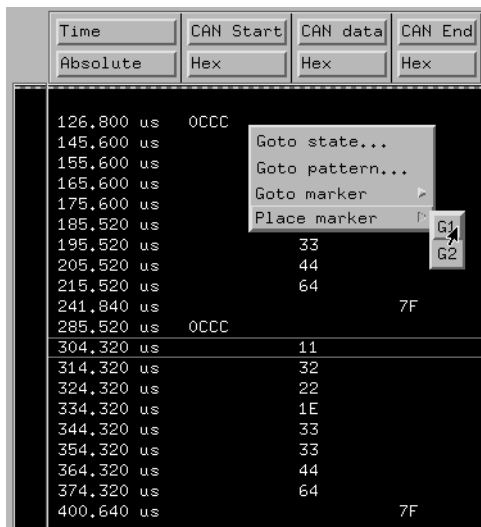
Now, look at the output of the serial tool to verify that the correct data was placed on the CAN bus. Click one of the “Navigate” buttons”, select “DemoTiming >”, and select “Listing<2>...” .

This listing is the output of the serial analysis tool. The listing shows the start block of the transmission (0CCC), the data transmitted, and the end block (7F). You see that the data fetched from memory was correctly transmitted on the CAN bus

8 Use global markers to correlate the captured data.

You can use the global markers to help you look at what the serial analysis tool is doing.

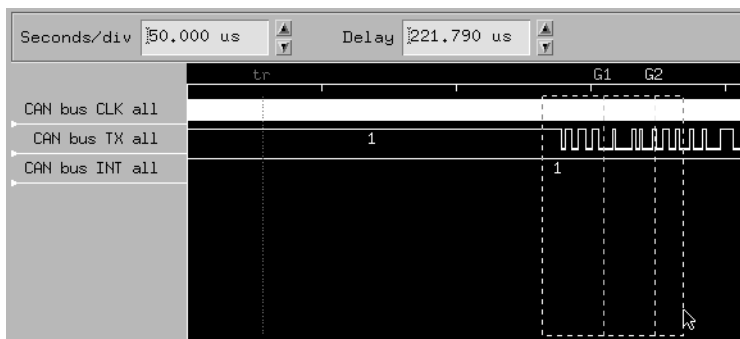
Right click in the listing area of the “Listing<2>” dialog. Select “Place Marker >” and “G1”.



Drag the G1 marker to just under the first 0CCC.

Place the G2 marker in the listing and drag it to just under the 11 in the data stream

Go to the “Waveform<2>” dialog. Place the pointer just to the left of the beginning of the CAN bus transmission. Click and hold the left mouse button and drag the left edge of the rectangle that was formed to a point just to the right of the G2 marker.



You now have an expanded view of the trace. You can see the form of the data transmitted on the CAN bus. (Keep in mind the CAN bus protocol specifies that a 0 gets added, or *stuffed*, after five 1s and a 1 gets stuffed after five 0s.)

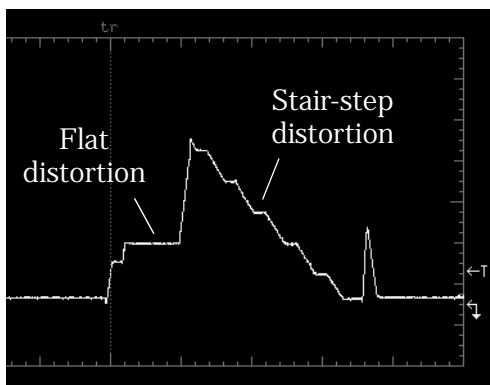
Summary

By looking at different areas in a target system and by correlating the captured data, you can view the flow of data from one part of the target system to the next.

Tracking hardware problems to their software causes

You can identify a problem with an analog signal using an oscilloscope module, trigger a logic analyzer module tracing software execution, and correlate the captured data to identify the cause of the problem all the way to the source code.

For example, the demo board's MPC860 processor has been programmed to generate a triangular waveform from a D/A converter, but the oscilloscope module shows problems with the waveform.

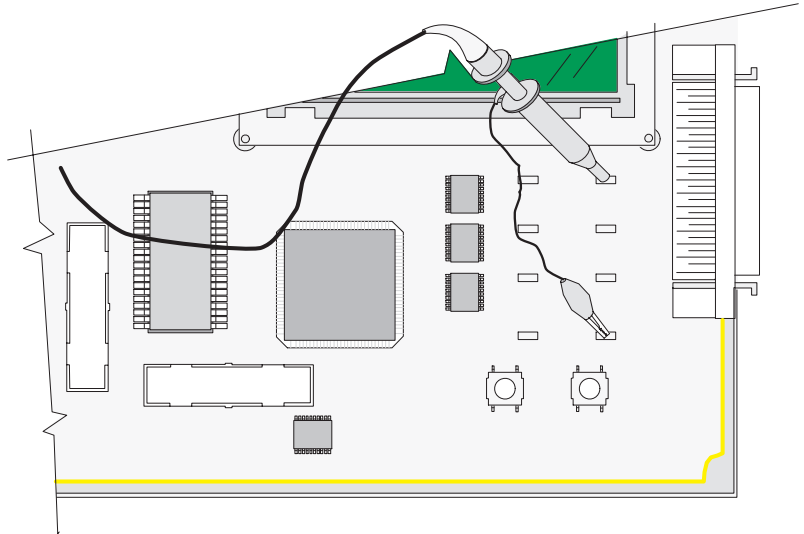


There are two problems with the triangular waveform: when the voltage is flat for approximately 350 microseconds, and when the voltage is flat for shorter times in varying numbers and duration, leading to a stair step effect.

- 1 Connect the logic analyzer, emulation module, and oscilloscope to the demo board.

Follow the instructions in the “Getting Started” chapter on page 9 for connecting the logic analysis module to the demo board.

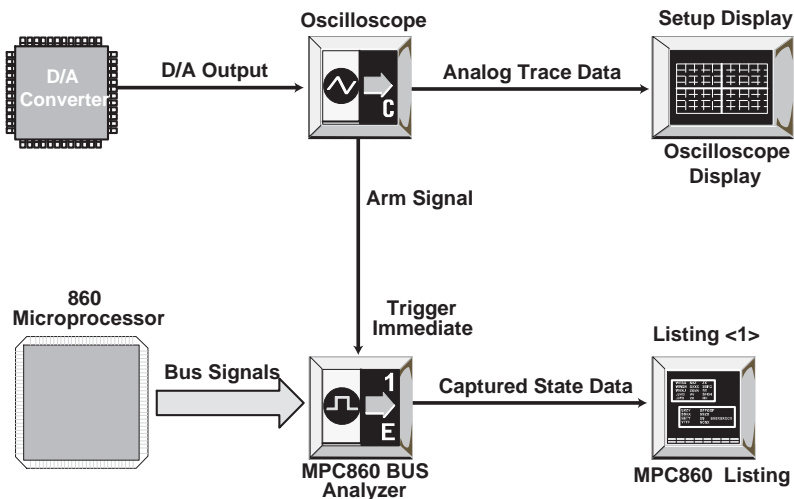
Also, connect the channel 1 oscilloscope probe to the D/A test point on the demo board. And, connect the ground clip to the GND test point.



NOTE:

Make sure the pattern generator data pods are not connected to the demo board; otherwise, the changes in demo program execution will affect the results of the measurements that follow.

2 Load the configuration files for this demo.



You will be loading the above configuration that will allow you to make a time-correlated measurement involving the oscilloscope and logic analysis modules. The oscilloscope module is configured to arm the logic analysis module when it triggers. The logic analysis module, in turn, is configured to trigger immediately when it is armed. This results in the two traces occurring at the same time and allows them to be time-correlated.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the `D_to_A.____` configuration file from the `/hplogic/demo/860_demo_board/configs/hp1670x` directory, and click the Load... button.

In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

- 3** Make sure the MPC860 demo board processor is running in a known state.

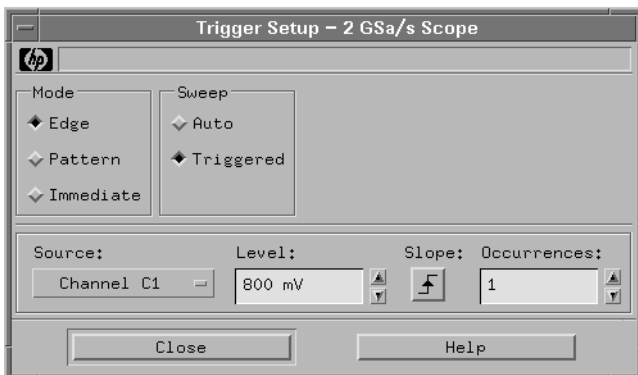
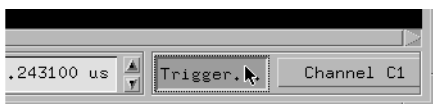
Click the “Reset”, “Break”, and “Run” buttons in order.



Resetting the processor starts it from a known state. Breaking puts the processor into the background monitor and allows the emulation module to read the microprocessor's configuration registers (whose contents enable breakpoints among other things).

4 Start the oscilloscope measurement.

Select “Trigger..” on the bottom of the oscilloscope display. Notice that the oscilloscope has been set up to trigger on an edge.



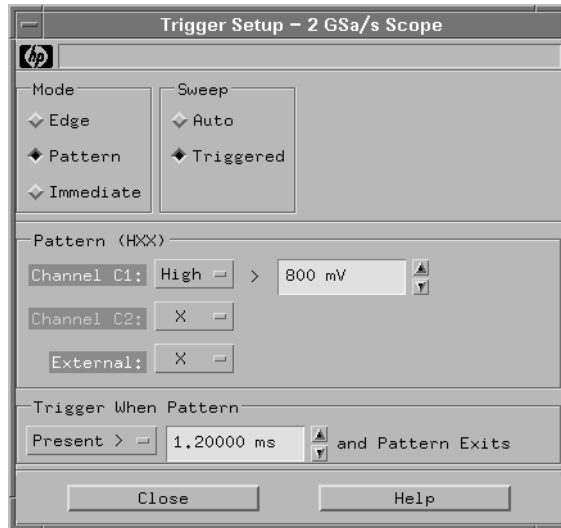
Click the “Group Run” button to take a trace and view the triangular waveforms. You should see the “flat distortion” defect, but you may not see the “stair step” distortion because it is very intermittent.

Click “Group Run” to view the captured waveforms a few more times. You see that the triangular waveform goes through various forms, from mildly distorted to heavily distorted. Notice that the heavily distorted triangular waveforms are infrequent.

5 Modify the oscilloscope trigger.

Now, set up the oscilloscope to trigger on a heavily distorted waveform. Go to the “Trigger Setup - 2 Gsa/s Scope” dialog by selecting “Trigger..”; then, select the “Pattern” radio button.

The pattern trigger has already been setup for a waveform that stays above 800 mV for more than 1.2 msec.



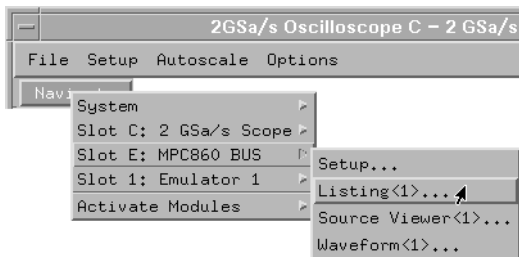
Click “Group Run” to capture one of the heavily distorted waveforms. (It may take several seconds because the waveforms are so infrequent.)

If the oscilloscope does not trigger, it may be because of variations in the demo boards. Shorten the period of the pattern trigger to capture a less distorted version of the waveform.

Close the trigger dialog to get it out of the way

6 Open the Listing and Source Viewer displays.

Click the “Navigate” button, select the “MPC860 BUS >” option, and select “Listing<1>...”.



Click the “Navigate” button again, select the “MPC860 BUS >” option, and select “Source Viewer<1>...”.

Move the Listing<1> window to the lower right hand corner of the screen and the Source Viewer window to the upper left hand corner of the screen to get them out of the way.

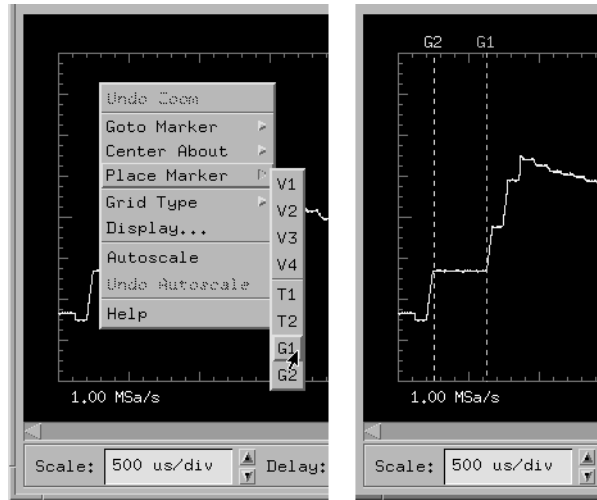
7 Use global markers to correlate the captured data.

Global Markers

The logic analysis system provides timing markers that span any modules that have been correlated. Placing a marker in the display of one module positions an identical marker at the correct time position in all correlated module displays.

Now, mark off the 350 microsecond (approximately) flat distortion with the global markers. Right click on the oscilloscope trace and select “Place marker >” and select “G1”. Don’t worry about getting the marker in exactly the right place at first, because they can be dragged into place after they appear. Place the G1 marker just past the end of the 350 microsecond (approximately) stretch in the triangular waveform. Place the G2 marker just before the beginning of the stretch.

Note that the inverse assembled listing has now moved to the location of the code that was executed at the G2 marker.



PC	MPC821/860 Inverse Assembler	
Symbols	10=hex, 10.=decimal, %10=binary	
	D/A control (CS5)	write 64
	proc_specifi+0238	addi r6 r6 000A
	proc_specifi+023C	andi r6 r6 00FF
	/q.elf:reset+0400	subi r1 r1 0080
	/q.elf:reset+0404	stmw r0 0000(r1)
	/q.elf:reset+0408	mf spr r26 srr0
	/q.elf:reset+040C	mf spr r27 srr1
	/q.elf:reset+0410	mfc r r28
	/q.elf:reset+0414	mf spr r29 lr
	/q.elf:reset+0418	mf spr r30 ctr
	/q.elf:reset+041C	mf spr r31 xer
	/q.elf:reset+0420	subi r1 r1 0018
	/q.elf:reset+0424	stmw r26 0000(r1)
G2.	/q.elf:reset+0428	mf spr r26
	/q.elf:reset+042C	ori r26 r26 0002
	/q.elf:reset+0430	mtmsr r26
	/q.elf:reset+0434	subi r1 r1 0008
	/q.elf:reset+0438	bl q.:isr:ext_exception
	isr:ext_exception	mf spr r0 lr
	ext_exceptio+0004	stw r0 0004(r1)
	ext_exceptio+0008	stwu r1 FFF8(r1)
	ext_exceptio+000C	lis r12 0000
	ext_exceptio+0010	lwz r11 4004(r12)

Bring the Source Viewer to the front and then bring the processor trace listing to the front. As you scroll through the processor trace listing, watch the Source Viewer. You see the source code move from running D/A code at the G2 marker to

servicing CAN interrupts. It will pass through the CAN service routine twice. You may have to back up a bit to get into the section of code that writes to the D/A controller. This is because it is difficult to place the marker precisely at the beginning of the flat distortion.

When you go past the G1 marker, you see the code go from the CAN service routine back to the main loop, which updates the D/A. You may also see the IRQ3 service routine execute while you are scrolling.

Summary

You can see that the CAN interrupt postpones the updating of the D/A voltage for over 350 microseconds. If the D/A update was considered more important than the CAN controller, you could modify the code to give priority to the D/A controller.

You can go through the same procedure to identify the cause of the smaller stair step distortions in the D/A output signal. By placing the G1 marker at the end of one of the stair steps, placing the G2 marker at the beginning, and scrolling through the listing, you can see that IRQ3 servicing is responsible for stair step effect.

See Also

“Controlling and modifying processor execution” on page 72. There you will turn off interrupts and observe the effect on the D/A waveform.

Tracking software problems to their hardware causes

When software execution behaves in a way that doesn't seem logically possible, you may have to look beyond the logical (digital) behavior of the system to the physical behavior, for example, by looking at the analog parameters of signals. If you can capture a software execution problem with the logic analyzer, you can also capture oscilloscope data from the target system at the same time, and you can correlate the captured data using global markers.

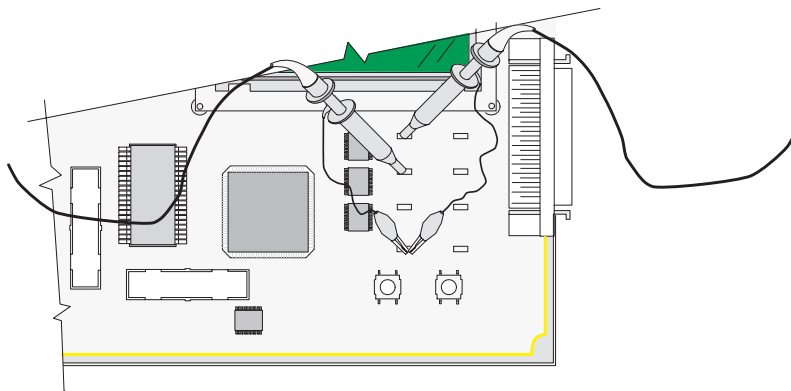
For example, in the MPC860 demo board's program code there are instructions that should never execute. However, if you set up the logic analyzer to trigger on them, you'll find that they do execute. You can set up a correlated measurement to capture data with the oscilloscope at the same time, and you can use global markers to correlate the captured data and discover the hardware cause of the problem.

- 1** Connect the logic analyzer, emulation module, and oscilloscope to the demo board.

Follow the instructions in the "Getting Started" chapter on page 9 for connecting the logic analysis module to the demo board.

Connect the channel 1 oscilloscope probe to the "D0 BOUNCE" test point on the demo board, and connect its ground clip to the GND test point.

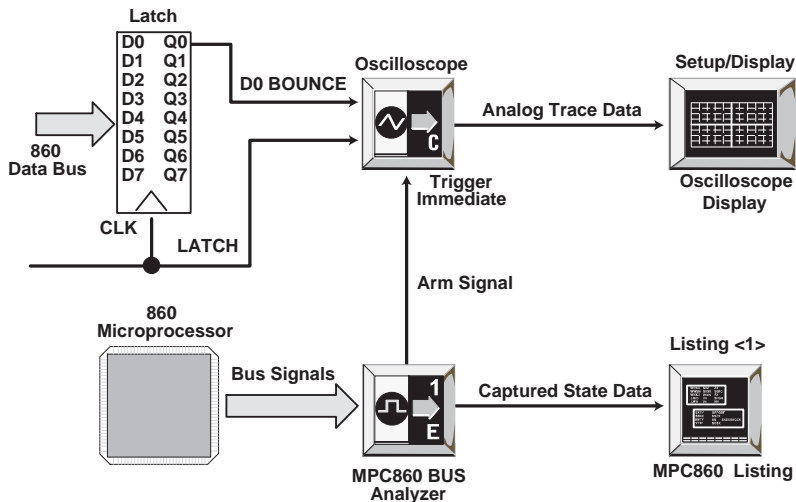
Connect the channel 2 oscilloscope probe to the "LATCH" test point on the demo board, and connect its ground clip to the GND test point.



NOTE:

Make sure the pattern generator data pods are not connected to the demo board; otherwise, the changes in demo program execution will affect the results of the measurements that follow.

2 Load the configuration files for this demo.



You are loading the above configuration. The logic analyzer arms the oscilloscope which then triggers immediately. This

allows the oscilloscope to capture what is happening on the D0 and LATCH lines at the time of the event the logic analyzer triggers on.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the Register.____ configuration file from the /hplogic/demo/860_demo_board/configs/hp1670x directory, and click the Load... button.

In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

3 Make sure the MPC860 demo board processor is running in a known state.

Click the “Reset”, “Break”, and “Run” buttons in order.



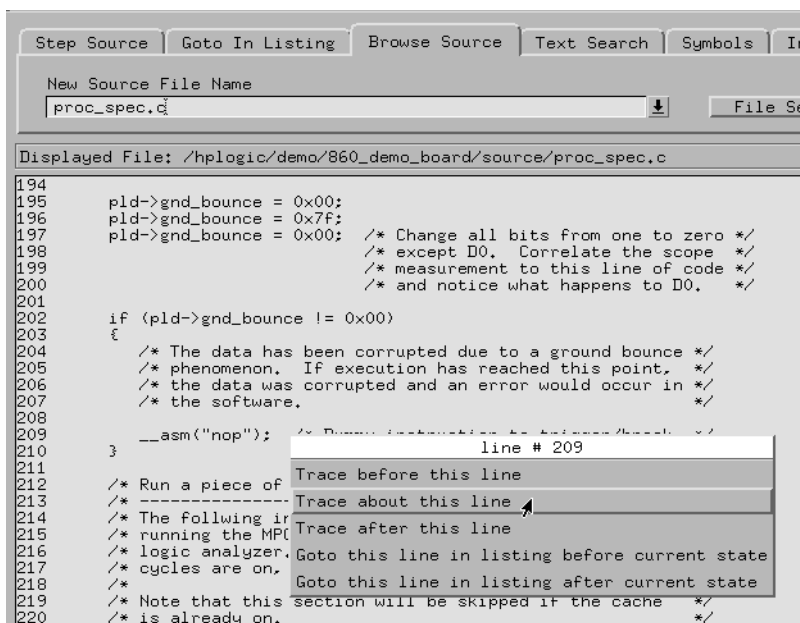
Resetting the processor starts it from a known state. Breaking puts the processor into the background monitor and allows the emulation module to read the microprocessor’s configuration registers (whose contents enable breakpoints among other things).

4 Set up to trigger on the software execution problem.

First take a look at the code where the problem is happening. Go the Source Viewer, select the “Browse Source” tab, select “File Selection...”, and select the file /hpllogic/demo/860_demo_board/source/proc_spec.c.

Scroll down to line 195. What you see is three lines that write 0x00, 0x7f, and 0x00 into a register. When the register is read after these writes, it should contain 0x00. The next line of code checks to see if 0x00 is in the register and goes to a NOP on line 209 if it is not. The code should never get to the NOP if the value in the register is 0x00 like it should be.

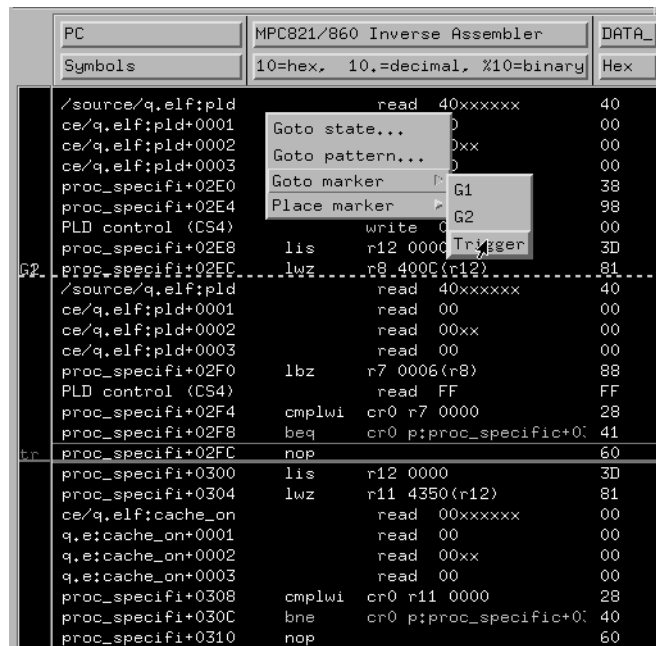
We can check to see if the microprocessor executes the NOP by setting the logic analyzer to trigger on it. Select line 209 and click on it. Select “Trace about this line” from the options.



- 5 Click one of the “Group Run” buttons to start the measurement.
- 6 Display the captured data.

After the trace has been taken, go to the microprocessor bus listing. Try scrolling the listing up and down. The source code highlight tracks the listing.

If the trigger is not in the center of the listing, right click on the listing, select “Goto Marker >”, and select “Trigger”. This places the trigger point in the center of the listing.

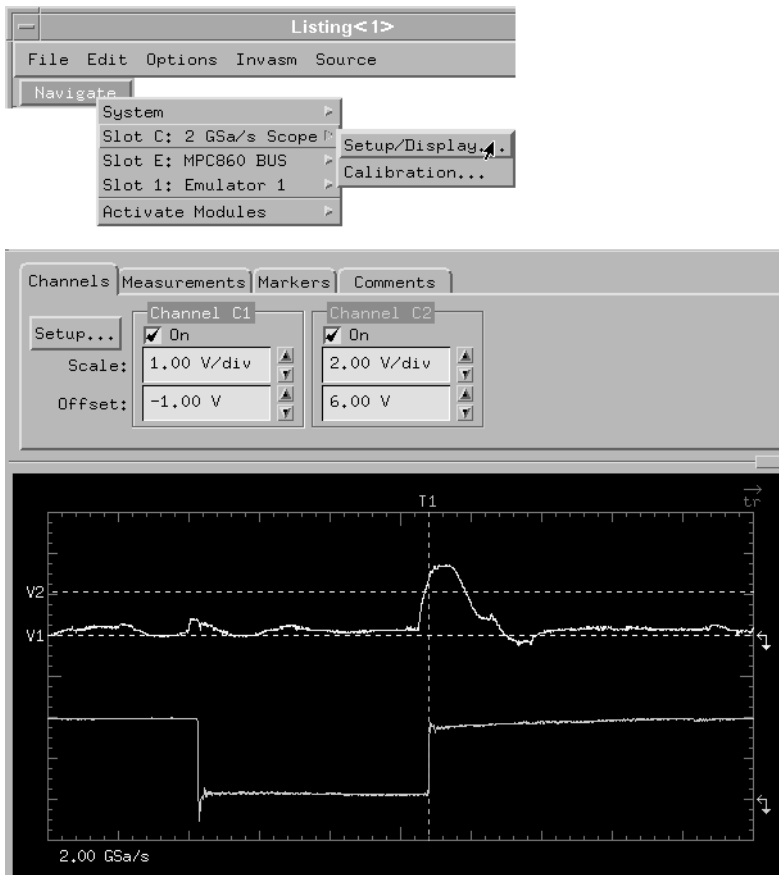


Notice the logic analyzer triggered on the NOP; this means the register did not contain 0x00. The question now is why.

- 7 Open the oscilloscope display.

Click one of the “Navigate” buttons. Select the “2 Gsa/s Scope” option and select “Setup/Display...”. The yellow channel 1 trace

is the register's D0 line and the green channel 2 trace is the register's clock line.



The oscilloscope has been set to trigger immediately when the logic analyzer triggers, so the trace you see is correlated to the microprocessor bus listing. The oscilloscope is set up to check the waveform of the D0 line when it is latched.

You can see, with the help of the timing marker and voltage marker, that the D0 line is at a logic 1 voltage level when data is latched into the register by the rising edge of the clock.

8 Use global markers to correlate data.

You can establish what code was executing when this happened by using the global timing markers.

Right click on the oscilloscope display, select “Place Marker >”, and select “G1”. Drag the G1 marker to the rising edge of the clock signal.

Now, go to the Listing<1> window and right-click in the black listing box. Select Goto Marker and G1. This will center the listing on the G1 marker.

Notice that this corresponds to the last of the three writes to the register. This means that a 0x00 did not get written into the register as it should have.

PC	MPC821/860 Inverse Assembler	
Symbols	10=hex, 10.=decimal, %10=binary	
/source/q.elf:pld		read 40xxxxxx
ce/q.elf:pld+0001		read 00
ce/q.elf:pld+0002		read 00xx
ce/q.elf:pld+0003		read 00
proc_specifi+02E0	li	r0 00000000
proc_specifi+02E4	stb	r0 0006(r9)
G1 PLD_control (CS4)		write 00
proc_specifi+02E8	lis	r12 0000
G2 proc_specifi+02EC	lwz	r8 400C(r12)
/source/q.elf:pld		read 40xxxxxx
ce/q.elf:pld+0001		read 00
ce/q.elf:pld+0002		read 00xx
ce/q.elf:pld+0003		read 00
proc_specifi+02F0	lbz	r7 0006(r8)
PLD_control (CS4)		read FF
proc_specifi+02F4	cmplwi	cr0 r7 0000
proc_specifi+02F8	beq	cr0 p:proc_specific+0
proc_specifi+02FC	nop	
proc_specifi+0300	lis	r12 0000
proc_specifi+0304	lwz	r11 4350(r12)
ce/q.elf:cache_on		read 00xxxxxx

It is also worth noting that the three writes consisted of 0x00, 0x7F, and 0x00. This means that the MSB, which is D0 in this system, never should have transitioned from a logic 0 during any of the writes. Yet the oscilloscope trace shows a logic 1 right at the rising edge of the latch.

You can also explore this phenomenon further by going up to line 182 in the source code. Here you will find three writes that

consist of 0x00, 0x01, and 0x00. If you set the trigger to the NOP after these writes and run the analyzer, you will find that it will not trigger.

So, what does this mean? When we only transition a single bit, as in the one set of writes, the correct value is latched by the register. When we transition most of the bits, as in the other set of writes, the wrong value gets latched by the register. A likely cause is ground bounce that gets severe enough to cause problems when most of the bits transition. Let's investigate further.

9 Probe the register's ground, and re-run the measurement.

You can verify that ground bounce is the problem by connecting the channel 1 oscilloscope probe to the GND BOUNCE test point. This test point connects directly to the ground connection of the register.

Click "Group Run" to take a trace of the ground line and observe the ground bounce.

Use the oscilloscope's voltage markers to assess the severity of the ground bounce.

Summary

By looking at the analog values of a signal as well as the digital values and by correlating the captured data, you can see how software symptoms might be caused by a hardware problem.

Looking at Firmware Driver Issues

Being able to start and stop program execution, set up logic analyzer triggers at locations in source code, and modify processor register and memory contents helps you develop and debug firmware drivers faster.

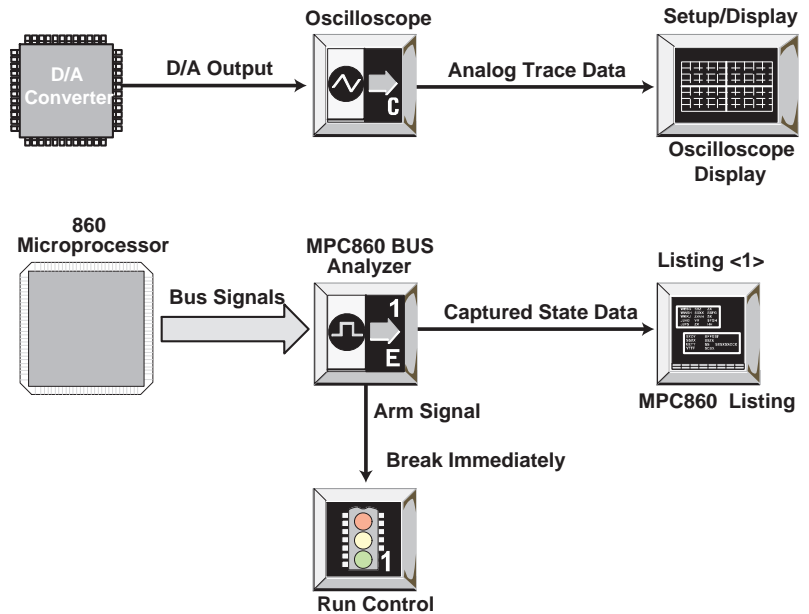
- By controlling the target system microprocessor's execution (run, stop, step, breakpoints), you can stop program execution at certain points and examine the state of your system.
- By using an HP emulation module, you can download code to target system RAM and execute it.
- By synchronizing stimulus to processor execution, you can begin the stimulus at an appropriate time.

Controlling and modifying processor execution

If your HP 16700A-series logic analysis system has an emulation module connected to a target system microprocessor's debug port, you can use the emulation module to start and stop the processor, and set breakpoints.

Normally you would use a Target Interface Module (TIM) to connect to the processor's debug port. In the case of the MPC860 demo board, however, the TIM is built in. Therefore, it has an emulation module connector right on the board, and you're able to control the MPC860 microprocessor execution using the emulation module.

The MPC860 demo board's D/A converter has a triangular waveform output signal with distortion caused by interrupts. In this demo, you will stop microprocessor execution, modify a microprocessor register to disable interrupts, continue microprocessor execution, and observe the effects on the triangular waveform.



The configuration you will load for this exercise arms the emulation (run control) module from the logic analyzer. This means that whatever the logic analyzer triggers on will cause a break in the processor's execution very close to that point. It is also important to note that the oscilloscope runs completely independently of any of the other instruments.

- 1 Connect the logic analyzer, emulation module, and oscilloscope to the demo board.

Follow the instructions in the “Getting Started” chapter on page 9 for connecting the logic analysis module to the demo board.

Connect the channel 1 oscilloscope probe to the “D/A” test point on the demo board, and connect its ground clip to the GND test point.

NOTE:

Make sure the pattern generator data pods are not connected to the demo board; otherwise, the changes in demo program execution will affect the results of the measurements that follow.

2 Load the configuration files for this demo.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the Turn_off_IRQ.____ configuration file from the /hpllogic/demo/860_demo_board/configs/hp1670x directory, and click the Load... button.

In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

The configuration file sets up the emulation module to stop microprocessor execution when the logic analyzer triggers.

3 Make sure the MPC860 demo board processor is running in a known state.

Click the “Reset”, “Break”, and “Run” buttons in order.



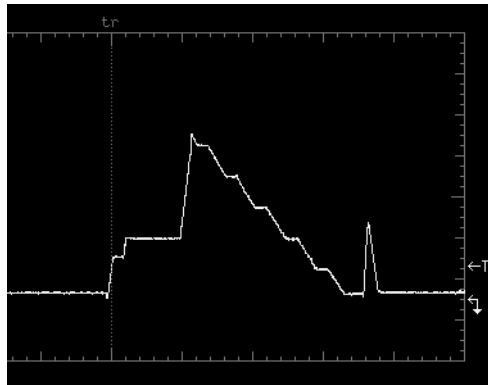
Resetting the processor starts it from a known state. Breaking puts the processor into the background monitor and allows the

emulation module to read the microprocessor's configuration registers (whose contents enable breakpoints among other things).

4 Display the triangular waveform's distortion.

In the first step of this measurement, you look at the analog triangular waveform generated by the D/A and processor.

To see that the form of the distortion varies over time, the oscilloscope is set up to run and trigger repetitively. In the "2G Sa/s Oscilloscope - Display" dialog, click the "Run(r)" button.



Let the oscilloscope trace the D/A repetitively for a while. You will see that you cannot get a true triangular waveform trace. Stop the oscilloscope trace, right-click the "Run(r)" button, and select "Single".

5 Look at the source code generating the triangular waveform.

Open the Source Viewer window by selecting Navigate, MPC860 BUS, and SourceViewer<1>.

In the Source Viewer dialog select the "Browse Source" tab and select "File Selection...". Select the file /hplogic/demo/860_demo_board/source/proc_spec.c file. Go to line 88, this is the line where IRQ3 gets enabled on each pass through the

proc_specific loop. IRQ3 is disabled towards the end of the proc_specific loop.

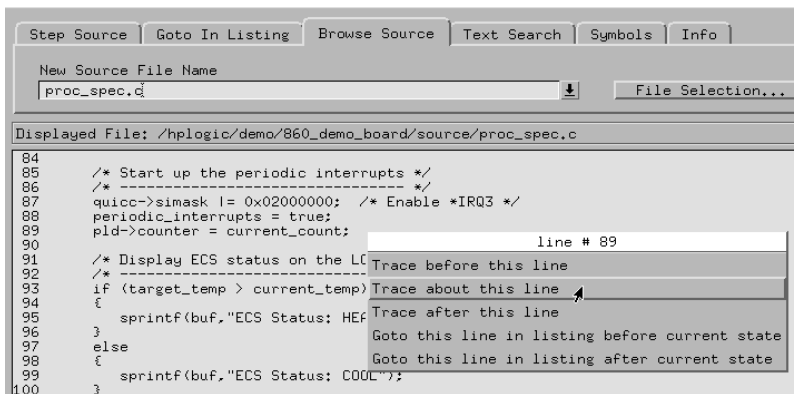
It is worth noting that IRQ2, the CAN interrupt and cause of the flat distortion, is only turned on during the demo board initialization. If it gets turned off, it stays off.

Now, go to lines 154 through 166 where you see the triangular waveform generation code.

If you would like more detailed information about what the Proc_specific loop does, go to “Demo Board Firmware” on page 143.

- 6 Stop processor execution just after IRQ3 is enabled (and before the triangular waveform generation code is executed).

In the “Source Viewer” window, click on line 89 and select “Trace about this line”. Click one of the “Group Run” buttons to start the analyzer trace.



```
84
85 /* Start up the periodic interrupts */
86 /* ----- */
87 quicc->simask |= 0x02000000; /* Enable *IRQ3 */
88 periodic_interrupts = true;
89 pld->counter = current_count;
90
91 /* Display ECS status on the LCD
92 /* ----- */
93 if (target_temp > current_temp)
94 {
95     sprintf(buf, "ECS Status: HEAT");
96 }
97 else
98 {
99     sprintf(buf, "ECS Status: COOL");
100 }
```

Displayed File: /hplogic/demo/860_demo_board/source/proc_spec.c

line # 89

Trace before this line

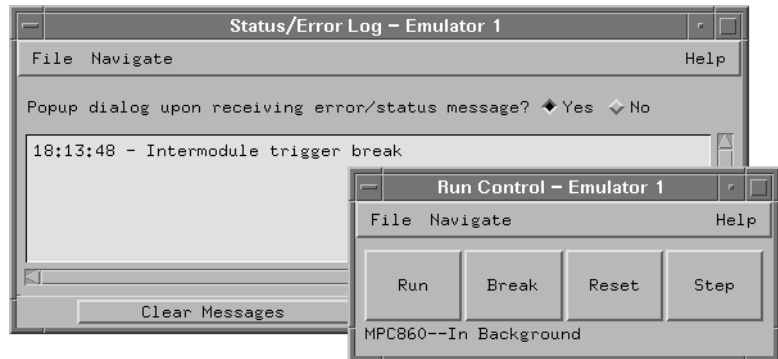
Trace about this line

Trace after this line

Goto this line in listing before current state

Goto this line in listing after current state

You get a status message that says there has been an “Intermodule trigger break”. This message, and the status line at the bottom of the “Run Control” dialog, inform you that the processor has stopped executing demo board firmware and is in the background monitor.



Click “Stop” to stop the trace measurement. (When processor execution stops, there are no states for the analyzer to capture and fill trace memory with, so the measurement does not complete).

You can verify where you are by looking at the processor trace in the “Listing<1>” dialog and at the correlated source in the Source Viewer window. Remember that the trigger must be centered in the listing display.

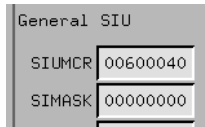
```
Displayed File: /hplogic/demo/860_demo_board/source/proc_spec.c
84
85 /* Start up the periodic interrupts */
86 /* ----- */
87 quicc->simask |= 0x02000000; /* Enable *IRQ3 */
88 periodic_interrupts = true;
89 pld->counter = current_count;
90
91 /* Display ECS status on the LCD */
92 /* ----- */
93 if (target_temp > current_temp)
94 {
```

7 Modify the SIMASK register to turn off interrupts.

Click a “Navigate” button, select “Emulator<1>”, and select “Registers...”. This dialog shows you selected registers of the processor and their values. The Registers dialog has been preconfigured to show only the SIU group.

Turn off interrupts by going to the SIMASK register, entering all 0’s, and then moving the cursor out of the SIMASK text window.

(Moving the cursor out of the text window causes the register change to take effect.)



8 Start the oscilloscope measurement.

Make sure the oscilloscope is not set to run repetitively.

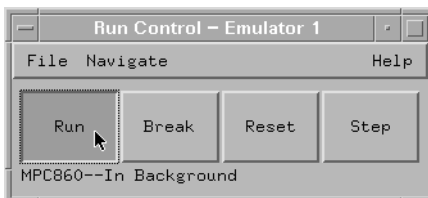
Click the green "Run" button on the oscilloscope.

The oscilloscope will not trigger until the processor is running because the D/A waveform will not be generated until then.

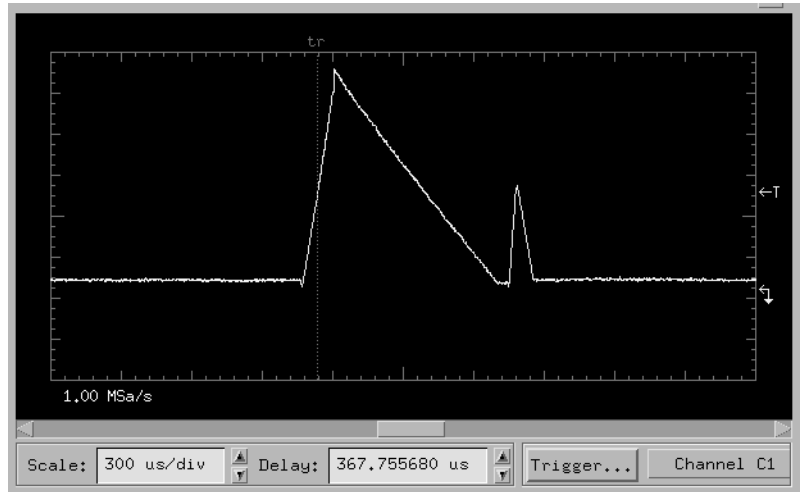
Also, note that the oscilloscope is not part of the group run associated with the analyzer. It is an independent instrument.

9 Continue processor execution.

In the Run Control dialog, click the Run button.



The oscilloscope should trigger almost immediately. What you get on the display is a “perfect” triangular waveform.



From this exercise, you can see that the defects in the triangular waveform were caused by interrupt service routines executing during the generation of the waveform.

10 Modify the SIMASK register to turn interrupts back on.

As the processor continues to run, IRQ3 will be turned back on again by code in the Proc_specific loop; however, the CAN bus interrupt will not. You can verify this by running the oscilloscope trace repetitively. You will not see the CAN bus flat spot, but you will see the IRQ3 stair step effect.

You can turn IRQ2 on again, along with other interrupts. Stop the processor in the proc_specific function by selecting one of the group runs. Now, go to the “Registers – Emulator 1” dialog, select the SIMASK text window, enter a 2a000000, and then move the cursor out of the SIMASK text window. Run the processor by clicking “Run” in the Run Control dialog.

Click the green Run button in the oscilloscope again to trace the triangular waveform repetitively; this will show the effect of the register change on the waveform.

Summary

Controlling the target system microprocessor's execution (run, stop, step, breakpoints) lets you stop program execution at certain points and examine or modify the state of your system.

Downloading code to RAM or Flash ROM

If your HP 16700A-series logic analysis system has an emulation module connected to a target system microprocessor's debug port, you can use the emulation module to download code to RAM or Flash ROM. Once code has been downloaded, you can use the emulation module to start the processor executing that code.

It is easy to quickly try out new or modified pieces of code on the target using the following procedure. Boot the processor and let the code in ROM initialize the system. Using the emulation module, break the processor, download the code, and change the PC to the start address of the code in RAM. Run the processor to execute the new code

For example, there is code located on the analysis system that you can download into RAM and start executing. The code will modify the message displayed on the LCD so that you will know it is running.

- 1** Connect the logic analyzer and emulation module to the demo board.

Follow the instructions in the “Getting Started” chapter on page 9 for connecting the logic analysis module to the demo board.

- 2** Load the configuration files for this demo.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the Download.____ configuration file from the /hplogic/demo/860_demo_board/configs/hp1670x directory, and click the Load... button.

In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

3 Set up the microprocessor for downloading code.

Reset, break, and run the processor, and wait until the LED stops flashing green. This ensures that the microprocessor has properly initialized.

Then, break the processor so it is not running when the download happens.

4 Load the executable file into RAM.

Select Navigate, then Emulator<1>, then “Load Executable...”.

Note that, in addition to downloading code into RAM, you can download code into Flash ROM or erase Flash ROM. Go ahead and explore these options if you would like. Note that the four main Flash algorithms are supported. Very few Flash ROMs do not support one of these algorithms. Before you continue be sure you return the “Operation” selection at the top of the dialog to “Load Executable”.

The file you are about to load is in Motorola S-record form, so it will automatically be loaded into the correct memory location. Note also that “Set PC after load” is selected. This means that when you hit run after the code is downloaded, execution will start at the beginning of the downloaded program. Select the “Browse...” button at the bottom of the dialog and select the file /hplogic/demo/860_demo_board/download/demo.srec. Select OK in the file browser dialog; then, select Apply and the file will be loaded. Click OK in the Load Completed dialog, and close the Load Executable window.

Now, look at the LCD display and you will see something like:

```
ECS Status: COOL  
Current Temp ##
```

5 Run the downloaded code.

Select Run on the Emulation dialog and note that the LCD display now says:

```
Running \
```

This comes from the code you just downloaded and verifies that it is executing.

6 Trace the code executing out of RAM.

You can now trace the code executing out of RAM. Click the green Run button in the Listing dialog. You will get a trace of the code executing in the demo board's RAM as well as a correlation to its source code.

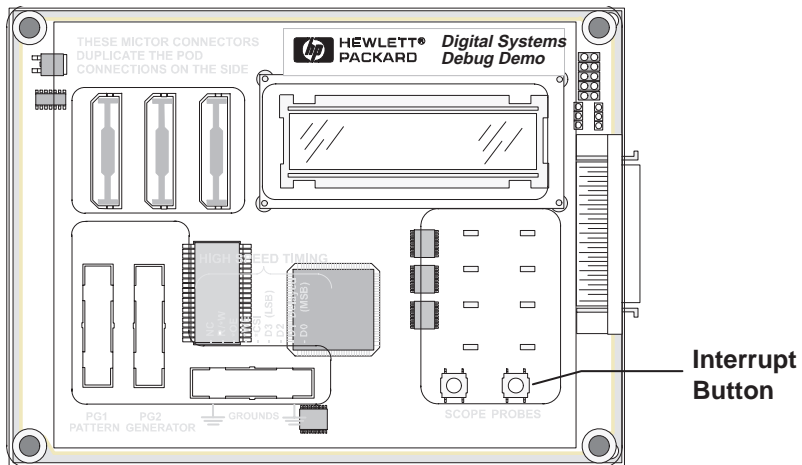
Summary

By using an HP emulation module, you can download code to target system RAM and execute it.

Synchronizing stimulus to processor execution

Sometimes sections of a target system under development are not complete or are not working properly. The pattern generator can be used to substitute for them. Often, it is useful to have the pattern generator generate vectors when a particular event has happened on the target system.

For example, the pattern generator can be used to write a message to the LCD display when an IRQ 1 is generated by pushing the Interrupt button.



NOTE:

You should do the exercise “Using the pattern generator” on page 111 first because it goes through the basics of the pattern generator.

1 Probe the MPC860 demo board.

Follow the instructions in the “Getting Started” chapter on page 9 for connecting the logic analysis module to the demo board.

If you have chosen not to do the exercise “Using the pattern generator” on page 111, follow its instructions for connecting the pattern generator very carefully.

Be sure to disconnect the pattern generator when you are done.

2 Load the configuration files for this demo.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the Trigger_Pat_Gen.____ configuration file from the /hpllogic/demo/860_demo_board/configs/hp1670x directory, and click the Load... button.

In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

3 Make sure the MPC860 demo board processor is running in a known state.

Click the “Reset”, “Break”, and “Run” buttons in order.



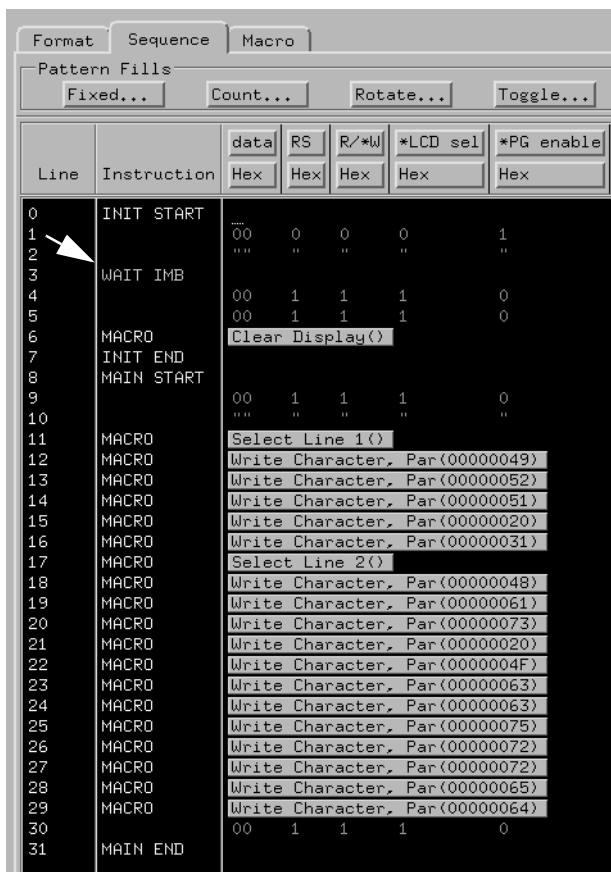
Resetting the processor starts it from a known state. Breaking puts the processor into the background monitor and allows the emulation module to read the microprocessor’s configuration

registers (whose contents enable breakpoints among other things).

4 Look at the pattern generator output sequence.

Go to the pattern generator dialog and bring it to the front.

The vector sequence you have loaded is a little different from the one you used in the first pattern generator exercise. First, the pattern generator will not execute most of the sequence until it receives an arm from the logic analyzer. This happens when the logic analyzer triggers.

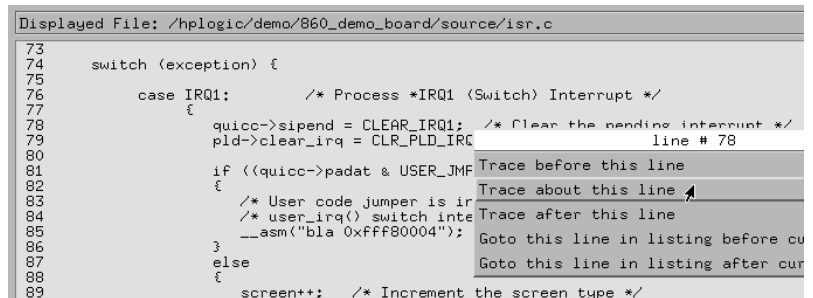


Second, the characters that will be sent to the display have been changed so a different message will be spelled out.

5 Set up the logic analyzer trigger.

To get the pattern generator to send the message to the display when an IRQ 1 is generated, the logic analyzer can be set to trigger when the IRQ 1 service routine is entered. The logic analyzer then arms the pattern generator, which causes it to send the vectors to the LCD display.

Go to the Source Viewer, select the Browse Source tab, select the File Selection... button, and view the /hpllogic/demo/860_demo_board/source/isr.c source file. Go to line 78 of the file which is where IRQ 1 get cleared, click on the line and select Trace about this line.



```
Displayed File: /hpllogic/demo/860_demo_board/source/isr.c
73
74     switch (exception) {
75
76         case IRQ1:          /* Process *IRQ1 (Switch) Interrupt */
77             {
78                 quicc->sipend = CLEAR_IRQ1; /* Clear the pending interrupt */
79                 pld->clear_irq = CLR_PLD_IRQ; line # 78
80
81                 if ((quicc->padat & USER_JMP
82                 {
83                     /* User code jumper is ir
84                     /* user_irq() switch inte
85                     __asm("bla 0xffff80004");
86                 }
87                 else
88                 {
89                     screen++; /* Increment the screen type */
```

The logic analyzer will now trigger when IRQ 1 is serviced.

NOTE: Close the Source Viewer window before going to the next step; otherwise, its search for source lines may interfere with the following measurement.

6 Run the measurement.

Go to the pattern generator dialog, and click Group Run.

The first two vectors of the sequence are generated, and now the pattern generator is waiting for the arm. The Run button has turned red and says Stop.

The *PG enable line has been set to high, so the LCD display should be updating.

Press the Interrupt button and the display should say the following:

*IRQ 1
Has Occurred*

If you click Group Run again, the display will begin updating again.

NOTE:

When you are finished with the exercise, be sure to disconnect the pattern generator.

Summary

By synchronizing stimulus to processor execution, you can begin the stimulus at an appropriate time.

Looking at Software Issues

Being able to make system performance measurements helps you analyze and validate application software.

- By using the HP B4600B system performance analysis (SPA) tool set, you can identify and characterize your target system's performance.
- By using the cache-on execution tracking inverse assembler, you can trace MPC860 processor execution when caches are turned on.

Analyzing system performance

You can quickly find the cause of performance problems in a section of code by using the HP B4600B system performance analysis tool set (also known as the SPA tool set).

This demo uses the SPA tool set to identify an occasional performance problem with a section of code executing on the MPC860 demo board. The SPA tool set is also used to identify the cause of the problem.

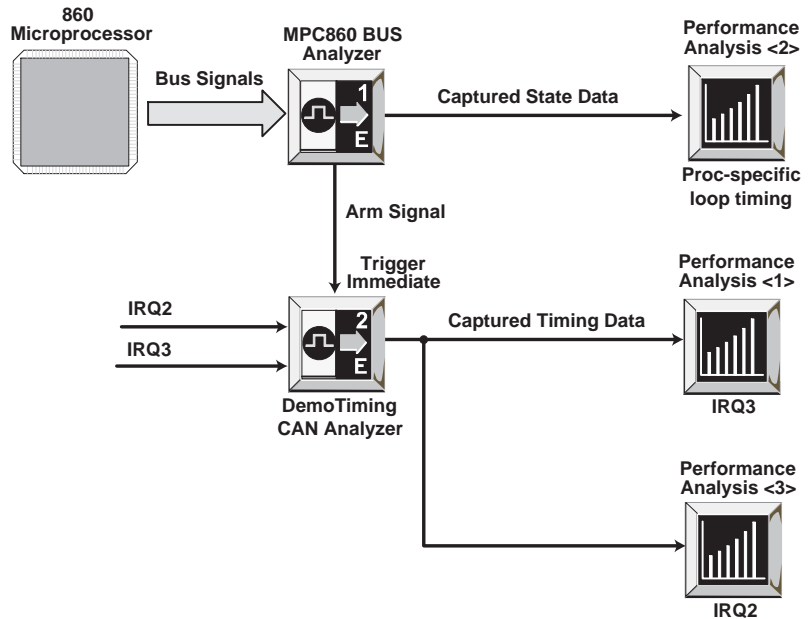
1 Probe the MPC860 demo board.

Follow the instructions in the “Getting Started” chapter on page 9 for connecting the logic analysis module to the demo board.

NOTE:

Make sure the pattern generator data pods are not connected to the demo board; otherwise, the changes in demo program execution will affect the results of the measurements that follow.

2 Load the configuration files for this demo.



You are loading the above configuration. The logic analyzer has been split into two virtual analyzers: one state to trace the MPC860 bus, and one timing to trace the IRQs. The outputs of both analyzers go to performance analysis tools.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the SPA.____ configuration file from the /hpllogic/demo/860_demo_board/configs/hp1670x directory, and click the Load... button.

In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

- 3** Make sure the MPC860 demo board processor is running in a known state.

Click the “Reset”, “Break”, and “Run” buttons in order.



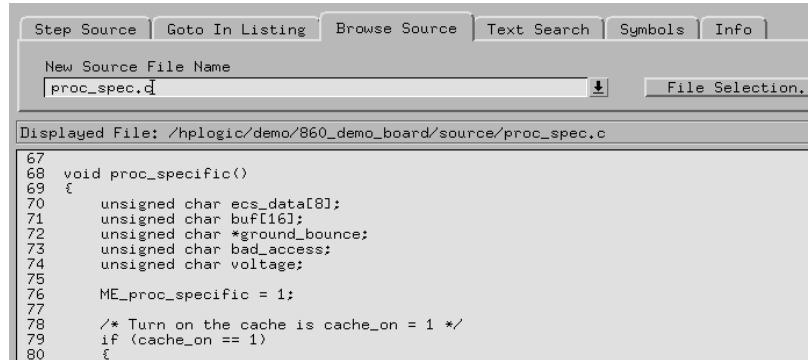
Resetting the processor starts it from a known state. Breaking puts the processor into the background monitor and allows the emulation module to read the microprocessor’s configuration registers (whose contents enable breakpoints among other things).

- 4** Review the source code.

Normally, for a measurement like this, you would be looking at code that you wrote. Since this is not the case, first load the code into the Source Viewer to review it.

Select the “Browse Source” tab, then select “File Selection...”, highlight the file `/hpllogic/demo/860_demo_board/source/proc_spec.c`, and select “OK”.

Go to line number 68 where `proc_specific` begins. On line 76 you see a write to the variable `ME_proc_specific`. This write is used to mark the beginning of `proc_specific`.



The screenshot shows a source code viewer window with the following content:

```
Step Source  Goto In Listing  Browse Source  Text Search  Symbols  Info
New Source File Name
proc_spec.d
File Selection
Displayed File: /hplogic/demo/860_demo_board/source/proc_spec.c
67
68 void proc_specific()
69 {
70     unsigned char ecs_data[8];
71     unsigned char buf[16];
72     unsigned char *ground_bounce;
73     unsigned char bad_access;
74     unsigned char voltage;
75
76     ME_proc_specific = 1;
77
78     /* Turn on the cache is cache_on = 1 */
79     if (cache_on == 1)
80     {
```

Go to line 275 and you see our end of loop marker, `MX_proc_specific`. You could have also found this line by using the “Text Search” tab.

NOTE:

Close the Source Viewer now as its search for source lines may interfere with the following measurements.

By using the logic analyzer to capture and store only writes to these two variables, you can observe the duration of the `proc_specific` loop over a large number of executions.

5 Set up the `proc_specific` performance measurement.

The processor trace has been set up to acquire 4K writes to these two variables. We could store many more of the writes, but 4K covers a span of 27 seconds, which is plenty for this exercise.

We have set up the system performance analysis tool to calculate the time duration between the pair of writes and to put them in buckets that are 1 millisecond in duration. This will tell us how much variation in the execution time of the `proc_specific` loop there is.

Open the first performance analyzer by selecting `Navigate, MPC860 BUS, and Performance Analysis<2>`. Move the dialog

to the lower right-hand corner of the screen. Close the Listing window (if visible) to get it out of the way.

You can see the time buckets down the far left side of the chart in the black area of the dialog. The tool shows what percentage of the marker pairs that were acquired has a duration that falls into each bucket.

6 Run the measurement.

Take a trace to see where the execution times fall. Click the green “Run” button. It will take about 30 seconds to get data in the chart. Most of this time is spent collecting the writes to the marker variables.

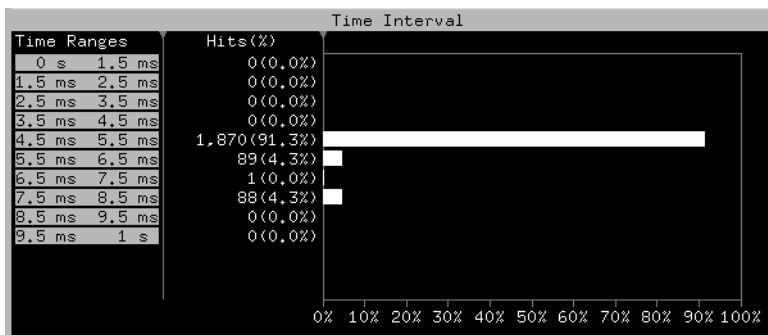
You will notice that the red “Stop” does not go away after data appears in the chart. This is because other data is still being processed in the background. We will get to that data momentarily.

NOTE:

DO NOT CLICK THE “STOP” BUTTON. If you already have, then take the trace again by clicking the green “Run” button.

7 Display the captured microprocessor bus data.

Look at the chart in the “Performance Analysis” dialog. You will see that most of the time intervals, about 90%, fall in the range of 4.5 ms to 5.5 ms. About 4% fall in the 5.5 ms to 6.5 ms range and about 4% fall into the 7.5 ms to 8.5 ms range.

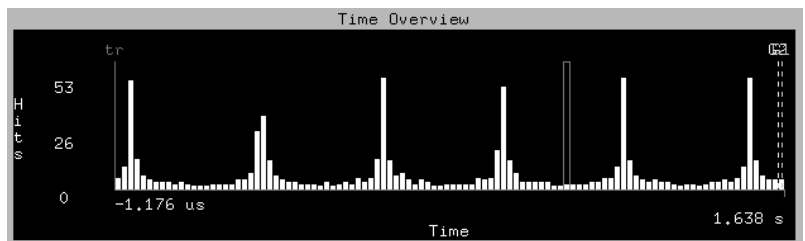


It is this last group of time duration that we will focus on. They represent a performance degradation of the `proc_specific` loop of 50%. We would like to know what is causing the degradation.

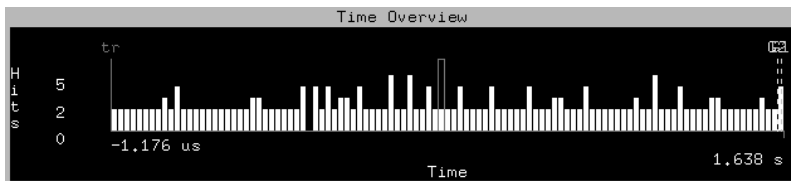
The `proc_specific` loop does not have a lot of different branches that it can execute. It basically executes the same code the same way for every loop. So we suspect that interrupts may be causing the degradation. For a complex system with a lot of interrupts, it might not be easy to determine which interrupt or interrupts were causing the problem. The demo board only has two interrupts active, not counting the interrupt initiated by the button next to the reset button. We will simulate locating this problem with these two interrupts.

8 Display the captured interrupt data.

Click the “Navigate” button, select `DemoTiming >`, and select “Performance Analysis<1>...”. This dialog contains a performance analysis of the number of occurrences of `IRQ3` over a period of about 1.6 seconds. The X axis of the chart is time, which spans from about 0 sec to about 1.6 sec. This time span has been divided up into 106 buckets and the number of `IRQ3`s that occurred during that time period (bucket) have been counted. As you can see `IRQ3`s sometimes occur very frequently and sometimes very infrequently.

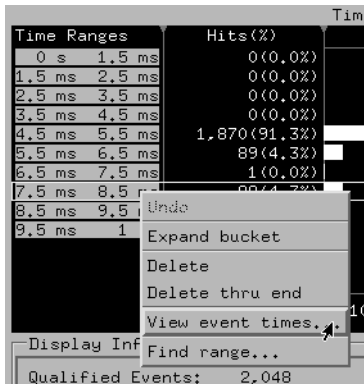


Go to navigate and get Performance Analysis<3>, which contains IRQ2 hits. You can see that IRQ2 is fairly consistent in the number of hits per time bucket.



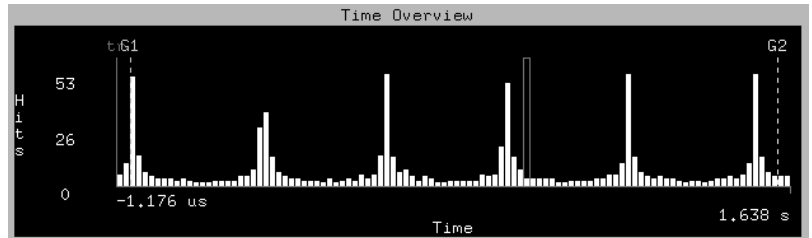
9 Use global markers to correlate the captured data.

To determine which IRQ is causing the problem, go to the Performance Analysis<2> dialog, proc_specific data, and right-click on the 7.5 ms to 8.5 ms bar and select “View event times...”. The dialog that pops up contains all the event times that were collected in that bucket.



Right-click on the first event times, select “Send start time to marker>”, and select “G1”. Look in the dialog that contains the IRQ3 data, Performance Analysis<1>.

You will see that the G1 global marker is right at one, probably the first, of the hit spikes in the IRQ3 data.



If you do the same with the rest of the event times that happen before 1.6 sec, you will see that the G1 marker lands right at one of the spikes in the number of hits. This tells us that it is likely that the performance degradation of `proc_specific` is due to the occasional large frequency of IRQ3s.

Summary

You have just seen how the performance analysis tool can be used to both identify a problem and find the cause.

Tracking processor execution with caches turned on

The MPC860 analysis probe provides a special execution trace inverse assembler that identifies branch trace messages generated by the MPC860 processor. This allows the Source Viewer to track source code even when the processor is executing out of cache memory.

For example, some of the MPC860 demo board's code is set up to execute out of cache memory. You can capture this execution, display it using the two kinds of inverse assemblers, and compare the Listing and Source Viewer displays.

1 Probe the MPC860 demo board.

Follow the instructions in the “Getting Started” chapter on page 9 for connecting the logic analysis module to the demo board.

2 Load the configuration files for this demo.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the Cache_off.____ configuration file from the /hplogic/demo/860_demo_board/configs/hp1670x directory, and click the Load... button.

In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

- 3 Make sure the MPC860 demo board processor is running in a known state.

Click the “Reset”, “Break”, and “Run” buttons in order.

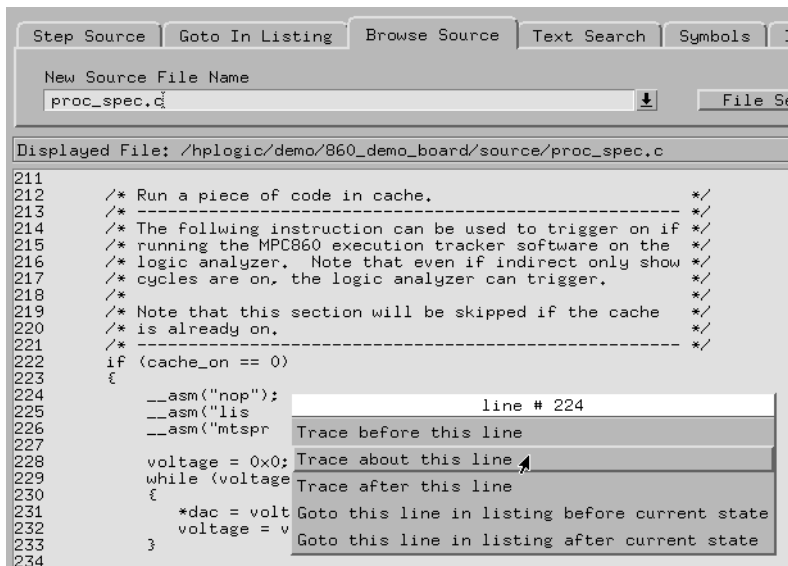


Resetting the processor starts it from a known state. Breaking puts the processor into the background monitor and allows the emulation module to read the microprocessor’s configuration registers (whose contents enable breakpoints among other things).

- 4 With the standard inverse assembler, look at executed code with caches turned on.

To set the analyzer trigger, go to the source viewer, select the “Browse Source” tab, select “File Selection...”, and select the file `/hplogic/demo/860_demo_board/source/proc_spec.c`. Scroll down to line 212. This is the beginning of the code that executes with cache on.

Set the analyzer to trigger about line 224, the NOP, and run the analyzer.



5 Display the captured data

When the trace has been taken, go to the “Listing<1>” dialog, and then go to the trigger point in the listing. You will see the assembly code being executed that turns off the cache. After that, things get strange. You will see the assembly code again because it was fetched into cache, and very shortly after that you will only see reads and writes to the D/A converter. Once the cache is turned on, following the code on the bus does not work very well.

Note also that the Source Viewer is unable to track the source code through this part of the inverse assembly.

State Number	PC	MPC821/860 Inverse Assembler
Decimal	Symbols	10=hex, 10.=decimal, %10=binary
0	proc_specifi+0310	nop
4	proc_specifi+0314	lis r20 0200
8	proc_specifi+0318	mtspr ic_cst r20
12	proc_specifi+031C	li r6 00000000
16	proc_specifi+0320	b p:proc_specific+0338
20	proc_specifi+0314	lis r20 0200
24	proc_specifi+0318	mtspr ic_cst r20
28	proc_specifi+0338	cmpwi cr0 r6 0080
32	proc_specifi+033C	blt cr0 p:proc_specific+03
36	proc_specifi+0340	li r6 00000080
40	proc_specifi+0334	andi. r6 r6 00FF
44	proc_specifi+0324	lis r12 0000
48	proc_specifi+0328	lwz r10 4014(r12)
52	proc_specifi+032C	stb r6 0000(r10)
56	proc_specifi+0330	addi r6 r6 000A
60	/source/q,elf:dac	read 50xxxxxx
61	ce/q,elf:dac+0001	read 00
62	ce/q,elf:dac+0002	read 00xx
63	ce/q,elf:dac+0003	read 00
64	D/A control (CS5)	write 00
65	/source/q,elf:dac	read 50xxxxxx
66	ce/q,elf:dac+0001	read 00
67	ce/q,elf:dac+0002	read 00xx
68	ce/q,elf:dac+0003	read 00
69	D/A control (CS5)	write 0A

6 Load the configuration files that use the execution trace inverse assembler.

Now load the configuration file “/hplgic/demo/860_demo_board/configs/Cache_on.____”.

This configuration is set up to use the execution trace inverse assembler.

The execution trace inverse assembler uses the MPC860’s branch trace messaging feature to follow processor execution when the caches are turned on.

7 With the execution trace inverse assembler, look at executed code with caching turned on.

Go to the source viewer, select the “Browse Source” tab, select “File Selection...”, and load the source file /hplgic/demo/860_demo_board/source/proc_spec.c.

Go to line 224 and set the trigger again.

Click the green Run button, and go to the “Listing<1>” dialog.

State Number	Sw_ADDR	MPC821/860
Decimal	Symbols	Cache-On Execution Tracker
0	proc_specifi+0310	Instruction Execution
16	proc_specifi+0314	Instruction Execution
32	proc_specifi+0318	Instruction Execution
53	proc_specifi+031C	Instruction Execution
101	proc_specifi+0320	Instruction Execution
102	proc_specifi+0338	Instruction Execution
150	proc_specifi+033C	Instruction Execution
151	proc_specifi+0324	Instruction Execution
199	proc_specifi+0328	Instruction Execution
202		4 byte Data Read = 504123D7H Address = ard/source/q,elf:dac
205		1 byte Data Read = 004123D7H Address = ource/q,elf:dac+0001
208		2 byte Data Read = 004123D7H Address = ource/q,elf:dac+0002
211		1 byte Data Read = 004123D7H Address = ource/q,elf:dac+0003
216	proc_specifi+032C	Instruction Execution
235		1 byte Data Write = 00H Address = D/A control (CS5)
240	proc_specifi+0330	Instruction Execution
244	proc_specifi+0334	Instruction Execution
248	proc_specifi+0338	Instruction Execution
252	proc_specifi+033C	Instruction Execution
254	proc_specifi+0324	Direct Branch Taken
258	proc_specifi+0328	Instruction Execution
263		4 byte Data Read = 504123D7H

You will now see the branch trace messages.

In the Source Viewer, you will be able to follow what source code was executed during this trace.

In this example, the section of code that executes out of cache is very short, but it demonstrates how source code could be tracked through a long section of code executing out of cache.

Summary

The execution trace inverse assembler makes it possible for the logic analysis system to provide source code correlation even when the processor is executing out of cache memory.

**Quickly Find the Cause of
Difficult Hardware Problems**

Capturing Very Deep Traces

Being able to capture very deep traces gives you the ability to capture widely separated causes and effects. You can also capture a large number of repeating events to help track down problems that might occur infrequently or to establish statistics of the event.

- By using logic analyzers that give you deep-memory traces, and by using the different types of filtering and display tools, you can capture a large amount of data (perhaps of a rarely occurring problem) and view the data in different ways without having to recapture it.

Using logic analyzers with deep memory

With HP's deep-memory logic analyzer modules, you can easily capture a trace of long duration and search it for a widely separated problem and its root cause.

For example, with the HP 16555D state/timing logic analyzer module and 2 million states of trace memory, you can capture 50 milliseconds of MPC860 demo board (25 Mhz) execution.

By contrast, you can capture 98 microseconds of MPC860 demo board execution with the HP 16550A state/timing logic analyzer module and 4K states of trace memory.

1 Probe the MPC860 demo board.

Follow the instructions in the “Getting Started” chapter on page 9 for connecting the logic analysis module to the demo board.

NOTE:

Make sure the pattern generator data pods are not connected to the demo board; otherwise, the changes in demo program execution will affect the results of the measurements that follow.

2 Load the configuration files for this demo.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the Deep_trace_____ configuration file from the /hplogic/demo/860_demo_board/configs/hp1670x directory, and click the Load... button.

In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

The Waveform<1> dialog that is brought up is set up to produce a timing trace of the microprocessor on the demo board. As you can see, the address and data buses are traced, as well as various status lines on the processor.

The analyzer has been set up to trace 2 million acquisitions of the 51 processor signals. As you will see, this is 50 msec of execution (at a sample rate of 41 MSa/s) of the processor running at 25 MHz.

For large traces such as this, 26 Mbytes, HP uses a demand-driven approach, which significantly speeds up the display of that data. Other logic analyzers will get bogged down displaying less data than is captured in this exercise.

3 Run the measurement.

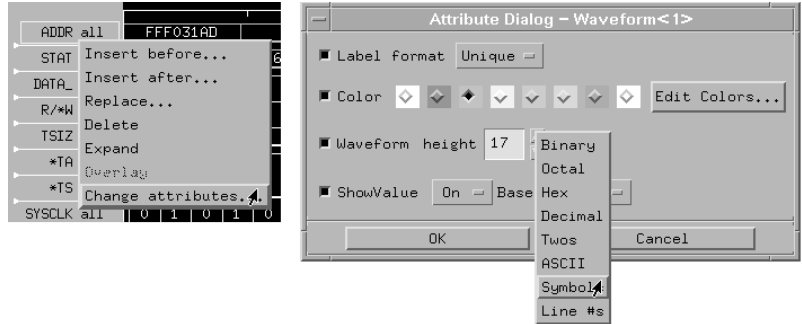
Click the green Run button to take a trace.

After the acquisition has completed, try moving around in the trace. Click on the scroll bar (because of the large trace, it is more of a dot than a bar), and drag it to the right or left. Notice how responsive the display is. This is a trace of bus cycles occurring during the execution of code on the demo board.

4 Display symbols in the captured data.

Symbols for the 860 processor were loaded into the analyzer with the configuration file you loaded. These symbols can be used in the trace as well. Right-click on “ADDR all” and select

“Change attributes...”. On the ShowValue line select “Hex”, pick “Symbols” from the pull down, and select “OK”.



The symbols for address that have been defined are displayed in the trace. To see more of the symbols, you can expand the display by decreasing the seconds per division.

5 Use the Goto tab to quickly go to certain locations.

You also have navigation aids. Select the “Goto” tab. Here you can quickly go to the beginning, trigger, or end of the trace.

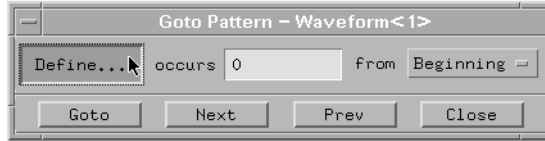


You can also place markers in the trace and go to them quickly.

6 Use the search capability to find particular data.

To place a marker at a specific address, the search feature can be used. We wish to find the first occurrence of an access to the

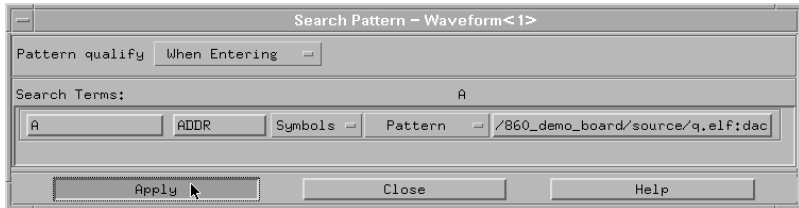
DAC. Select the “Search” tab, select “Advanced searching...”, and in the dialog that comes up select “Define...”.



We want to search for a symbol, so in the Search Pattern dialog select “Hex” and change it to “symbols”. Expand the dialog and select “Absolute XXXXXXXX”. The dialog that comes up shows the list of symbols read into the analyzer.

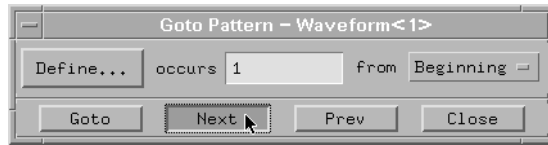
To narrow down the list deselect all of the types in the “Find Symbols of Type” box except for the “Variable” type. Click in the list box and scroll down until you find the “dac” symbol. Select it and click OK.

In the “Search Pattern” dialog, select “When Present” and change it to “When Entering”, then select “Apply”.



The waveform display has now gone to the 0th occurrence of the DAC address from the beginning, which is the beginning of the trace.

In the “Goto Pattern” dialog, select “Next”.



The trace will center on the first occurrence of an access to the DAC.

7 Use markers for easy return to points in the data.

Should you want to return to this position at a later time without using the search, you can place a marker here. Right-click within the ADDR trace where you want the marker placed. Select “Place marker >” and select “G1”. If the marker does not go exactly where you want, you can drag it into place.



One point is worth noting. If you compress the display, select the up arrow next to “Second/div”, more and more of the data acquired is being displayed. The more data displayed, the slower the trace will scroll.

Summary

By using logic analyzers that give you deep-memory traces, and by using the different types of filtering and display tools, you can capture a large amount of data (perhaps of a rarely occurring problem) and view the data in different ways without having to recapture it.

Creating Stimulus for Target Hardware

Being able to stimulate certain areas of your target system with test vector signals helps you test when hardware is not available or when you want to test your target system against certain types of interactions that may occur rarely in the real world.

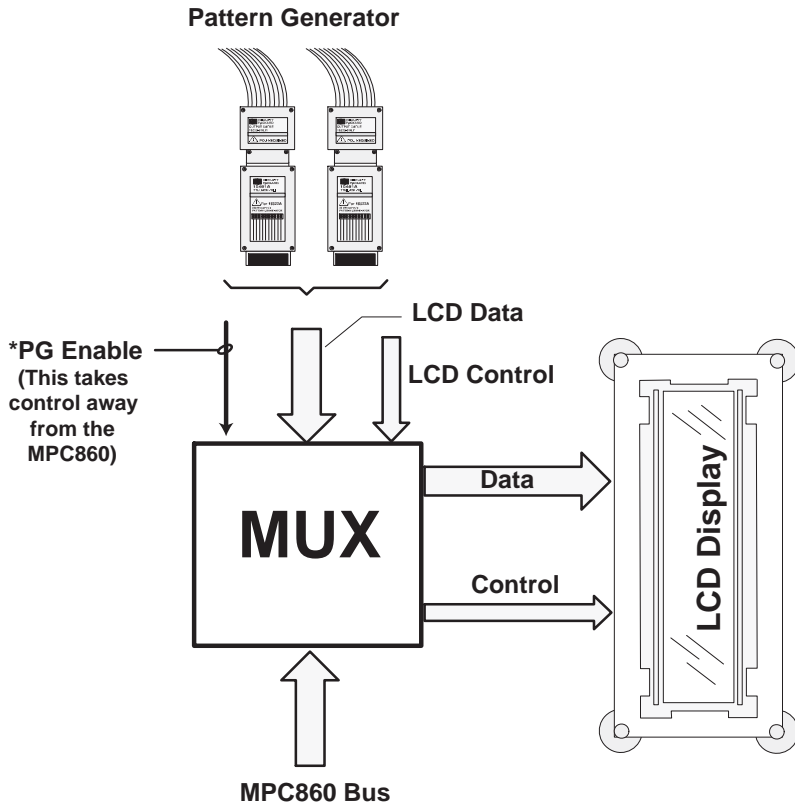
- By using the pattern generator module, you can check the functionality of your target system by stimulating various sections of it with preprogrammed vectors.

Using the pattern generator

The following exercise requires the HP 16522A pattern generator module. Your demo system may not have this module installed. To verify that the module is installed, go to the main logic analysis system window and look at the module buttons going down the left side. If the pattern generator module is installed, you will see a button for it.

With the pattern generator module, you can check the functionality of your target system by stimulating various sections of it with preprogrammed vectors. These vectors can even be correlated with other signals on the target system (see exercise “Synchronizing stimulus to processor execution” on page 84).

For example, with the MPC860 demo board, you can drive the LCD with the pattern generator.



As you can see, the LCD display on the demo board is connected to a multiplexer that allows the pattern generator to take control of it.

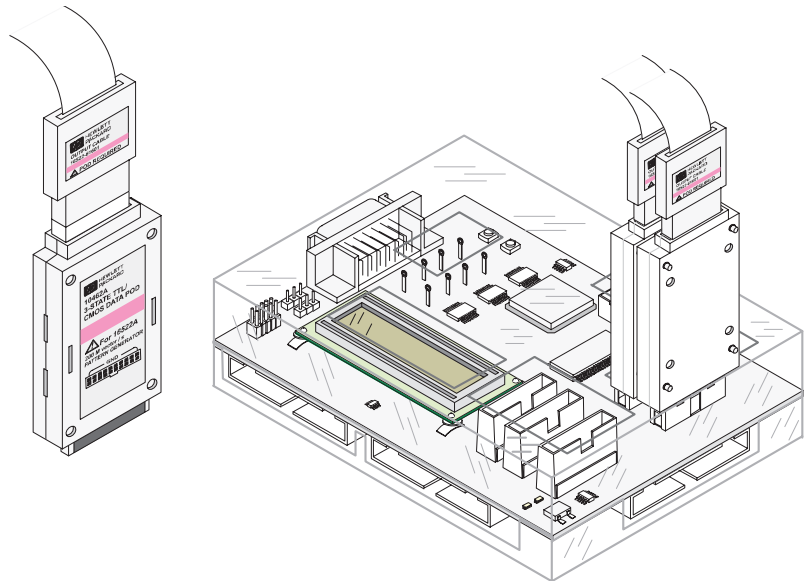
- 1 Connect the pattern generator outputs to the MPC860 demo board.

Make sure that the TTL data pods are attached to the pod 1 and 2 connectors at the end of the pattern generator cables. If the TTL data pods (HP 10461A) are missing, contact your FE to get them for you.

NOTE:

HP has made a variety of data pods available for the pattern generator. The data pods provide voltage levels for TTL, 3-state TTL/3.3v, 3-state TTL/CMOS, ECL terminated, or ECL unterminated. (The logic level without a data pod is differential ECL.)

Connect data pod 1, with a TTL data pod attached, to PG1 and data pod 2, with a TTL data pod attached, to PG2. Note that the pod 1 cable is the right-hand-most cable when facing the back of the analyzer.



When you connect the pods, it is likely that the LCD display will stop updating. This is because the default outputs of the pattern generator disconnect the LCD display from control of the demo board processor.

NOTE:

Having the pattern generator connected changes the timing of code executing on the demo board. This is because the processor cannot communicate with the display and retries 2,000 times every time it accesses the display. Make sure you disconnect the pattern generator from the demo board when you are done with this demo to prevent it from affecting other exercises.

2 Load the configuration files for this demo.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the Stimulus.____ configuration file from the /hplogic/demo/860_demo_board/configs/hp1670x directory, and click the Load... button.

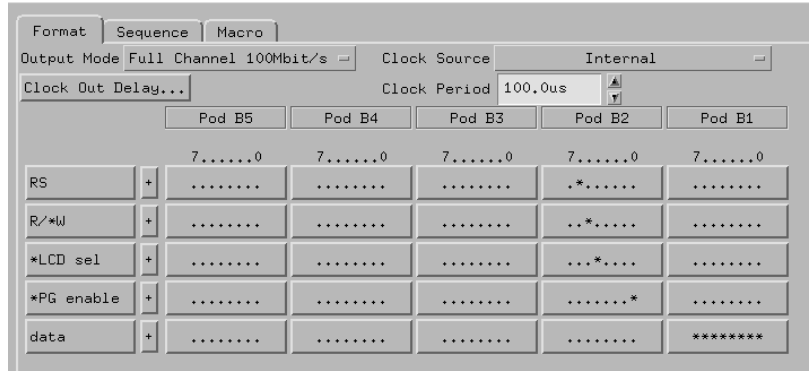
In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

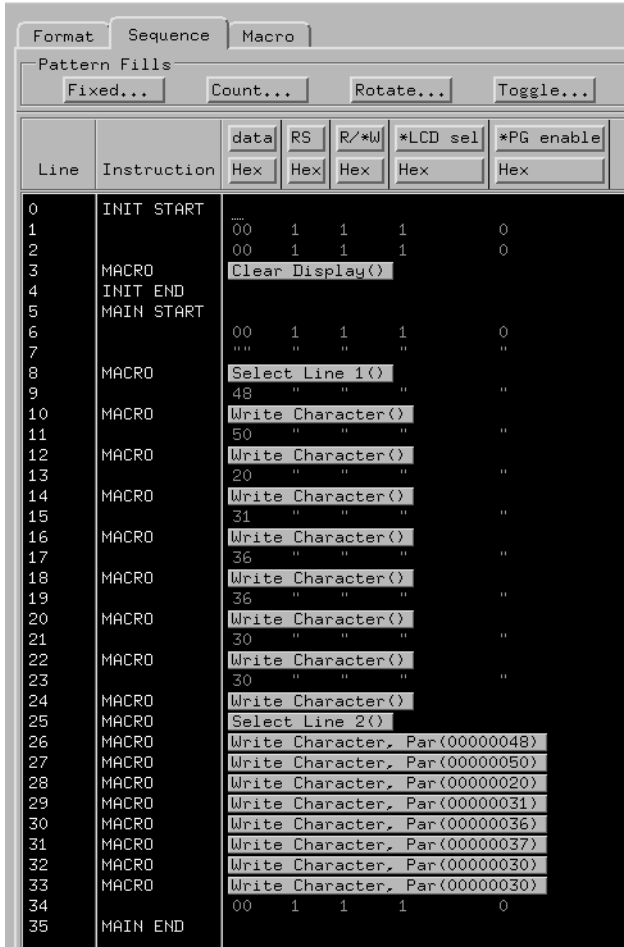
3 Look at the pattern generator format.

In the Format tab, you set the output clock rate, and you assign and name pattern generator outputs. Note the LCD data and control labels down the left side.



4 Look at the pattern generator output sequence.

In the Sequence tab, you can edit the pattern generator output sequence.



A sequence has been created for you that writes

HP 1660
HP 1670

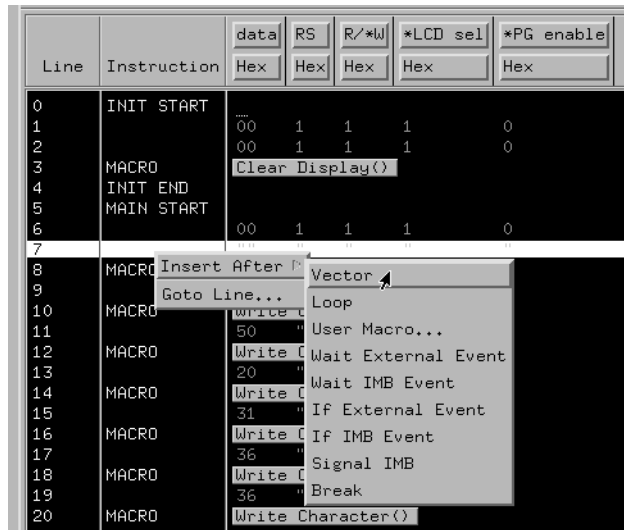
to the display.

This sequence consists of the following macros:

- Clear Display()
- Select Line 1()
- Select Line 2()
- Write Character()
- Write Character, Par()

The reason for the “Write Character, Par()” is to show how parameters can be used in macros. You will take a look at these macros a little bit later in this exercise.

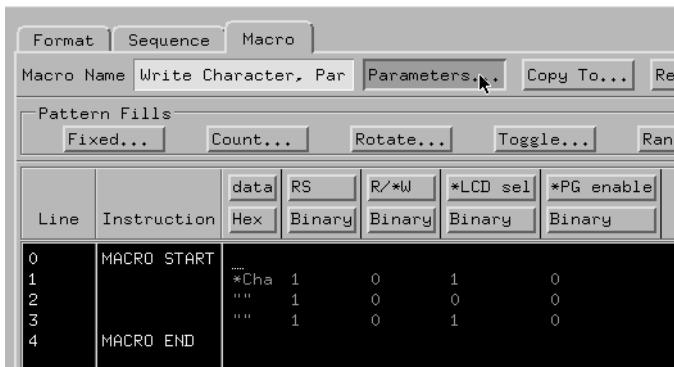
Use the popup menus to add to the pattern generator’s output sequence.



5 Look at the pattern generator macros.

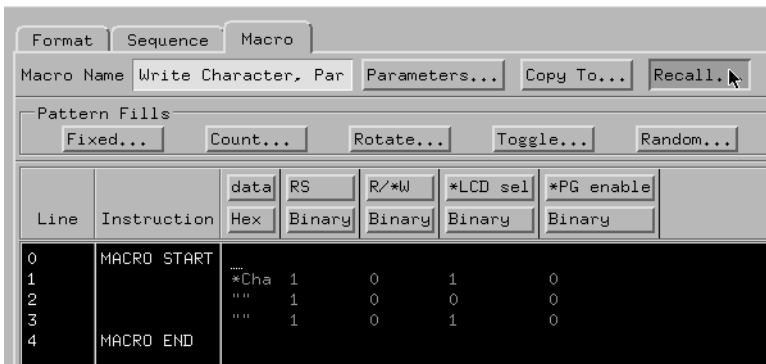
In the Macro tab, you set up patterns that can be repeated in the output sequence.

To define the parameters that can be used in a macro, click Parameters..., enter the parameter name, and turn the parameter on or off.



To use a defined parameter in a macro, right-click the location where you want to use the parameter and select “Set parameter...” from the popup menu.

To view the predefined macros discussed earlier, click Recall... and select the macro.



6 Run the pattern generator.

To cause the pattern generator to output its sequence of vectors, click the green Run button.

The output sequence defined by this example's configuration will write "HP 16600" to the first line, and "HP 16700" to the second line, of the demo board's LCD display.

NOTE:

Be sure to disconnect the pattern generator before leaving the exercise.

Summary

By using the pattern generator module, you can check the functionality of your target system by stimulating various sections of it with preprogrammed vectors.

Verifying Setup/Hold Violations

Being able to test for setup and hold violations on an entire bus helps you quickly verify whether your target system meets its design specifications.

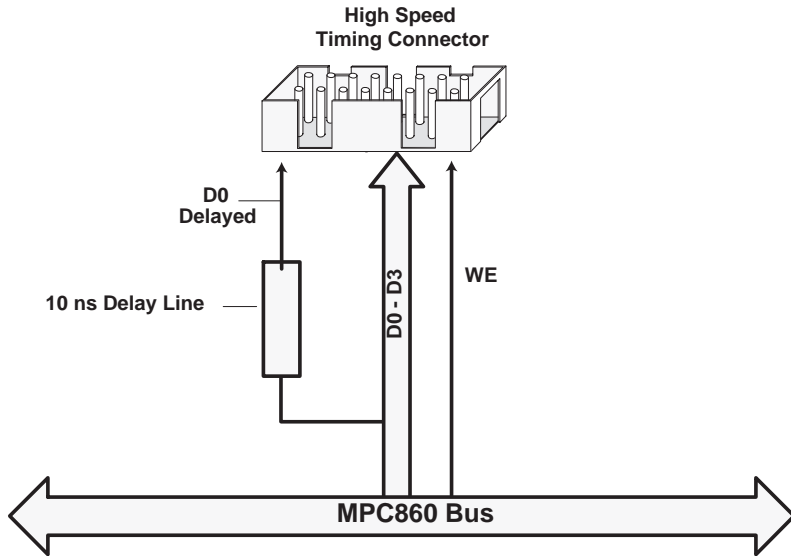
- By using the high-speed state/timing logic analyzer module, you can quickly verify setup and hold timing margins on any bus.

Using the high-speed logic analyzers

The following exercise requires the HP 16517A high-speed state/timing logic analysis module. Your demo system may not have this module installed. To verify that the module is installed, go to the main logic analysis system window and look at the module buttons going down the left side. If the high-speed logic analysis module is installed, you will see a button for it.

With the high-speed state/timing logic analyzer module, you can quickly verify setup and hold timing margins on any bus.

For example, in the MPC860 demo board a setup violation has been simulated. Four lines of the data bus, D0-D3, and some control lines have been routed to a connector for the high-speed analyzer. In addition, the D0 line has been delayed by 10 nsec and routed to the connector. Even though the delayed D0 is not part of a bus, it simulates a setup violation. You can use the HP 16517 high-speed timing logic analysis module to find that setup violation.



You will load a configuration that uses the setup and hold trigger macro available in the HP 16517.

You will verify that the D0 line of the data bus violates the 64 ns setup time of the data bus.

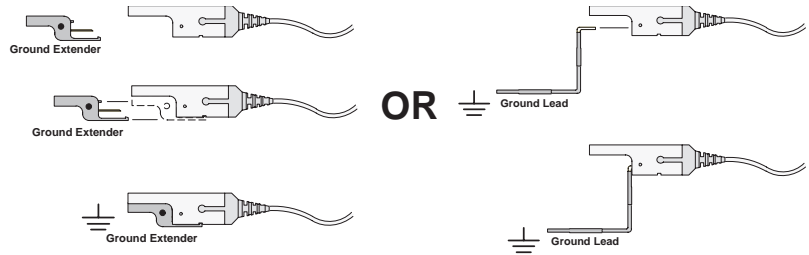
You will then move the D0 probe to the undelayed D0 signal and use the HP 16517 to establish the margin of the data bus.

1 Probe the MPC860 demo board.

Locate the HP 16517 master pod. Connect the probes of the master pod as follows:

Probe	Demo Board Connection
0	D0 Delayed
1	D1
2	D2
3	D3
4	WE

Use the 1/10 center ground adapter on at least two of the probes.



In this example we have only probed 4 lines of a data bus, the HP 16517 and HP 16518 modules can be combined to probe up to 80 signals with a skew of no more than 250 ps across all channels.

You need to have at least one of the logic analyzer pods connected to the demo board to provide power. If the 5 pods are connected from previous exercises, that is okay.

It is important that the emulation module cable is not connected as it can hold the processor of the demo board in reset, and it is necessary that the processor be executing for this exercise. Also, the pattern generator pods should be disconnected.

2 Load the configuration files for this demo.

In the main logic analysis system window, click the File Manager button.



In the File Manager dialog, select the Setup_Hold.____ configuration file from the /hplogic/demo/860_demo_board/configs/hp1670x directory, and click the Load... button.

In the Load Configuration dialog, click Load.

If a confirmation dialog appears, click Yes.

(You can also choose the File, Load Configuration... command from the menu bar of most windows.)

3 Make sure the MPC860 demo board processor is running.

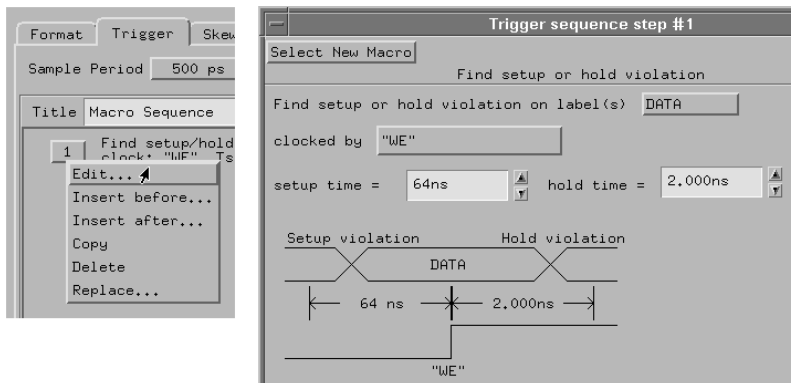
To make sure the demo board is in the proper configuration reset it by pushing and holding reset button for 2 seconds; then, wait until the green LED stops flashing.

4 View the trigger setup.

The data bus is latched on the rising edge of WE. Data on the data bus should be stable for 64 ns before the rising edge of WE and 2 ns afterwards.

To see the trigger setup, in the “4 GHz Timing/1 GHz State A - 4GHz/1 GHz” window select the “Trigger” tab. The center of this tab is the trigger sequence area, you will see one sequence.

Select the “1” button in front of the sequence and select the “Edit...” option. You will see a graphic depiction of the trigger macro you are about to use. The macro will trigger on any bus transitions that occur less than 64 ns before the rising edge of WE and less than 2 ns afterwards.



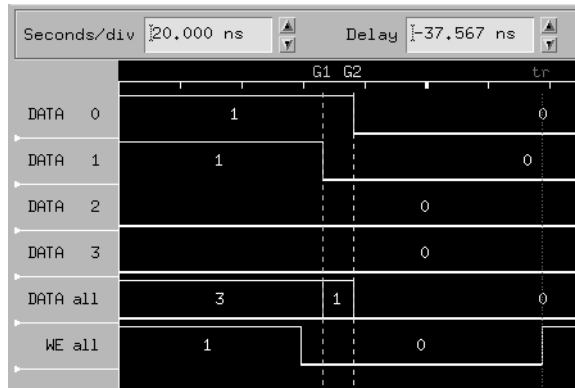
It is important to understand the implications of this measurement. When taking an oscilloscope or logic analysis trace, you are only looking at a very small part of a target's

overall execution time. This trigger looks at each and every rising edge of WE and verifies that the setup/hold you specified was not violated. If it is, the analyzer triggers and you get to see what happened.

Select “Cancel” to close the edit trigger sequence window.

5 Run the measurement.

Run the measurement by clicking one of the green “Run” buttons. You will see by the “DATA 0” measurement that D0 has been delayed from the other bits of the data bus.



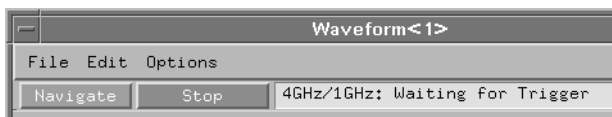
Set up the measurement to run repetitively by right-clicking on the green “Run” button and selecting “Repetitive”.

Run the measurement again. You will see that D0 is always delayed and that it is violating the setup time.

6 Probe D0, and run the measurement again.

To see that the undelayed D0 bit does not violate the setup time, move probe 0 from “D0 Delayed” to “D0” on the demo board.

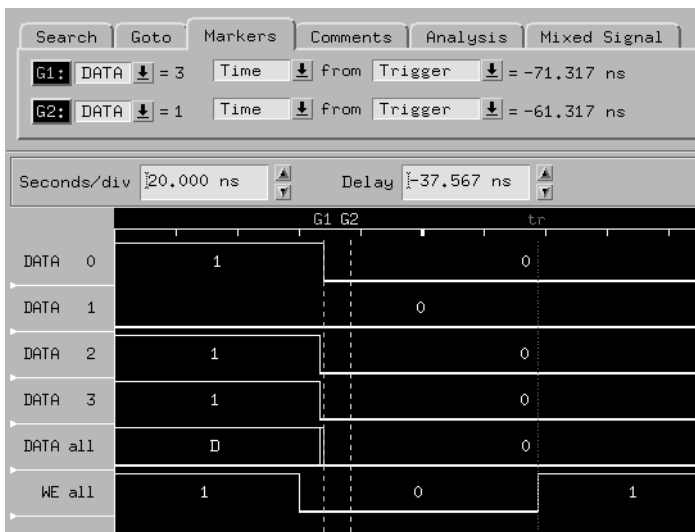
The analyzer will stop triggering.



Stop the analyzer, go back to the trigger menu, and edit the setup time to 70 ns and run the analyzer. Continue adjusting the setup time by increasing or decreasing it in 2 ns increments until you have established the value of the setup time in the trigger where the analyzer just triggers reliably. Note that when the analyzer doesn't trigger, you must stop the measurement before you can modify the trigger specification and run again.

Right-click on the D0 waveform, just before the trigger. Select "Place marker..." and select G1. Click and hold on the "G1" at the top of the display and slide the G1 marker until it is even with the last transition on the data bus.

Select the "Marker" tab and read the time difference between G1 and the trigger point. This is the setup time for the data bus for this measurement.



You could repeat this measurement several times to establish the worst case setup time and therefore how much margin from 64 ns you have.

Summary

With the high-speed state/timing logic analyzer module, you can quickly verify setup and hold timing margins on any bus.

A

About the MPC860 Demo Board

Demo Board Hardware

Introduction

The MPC860 demo board is a Motorola MPC860 PowerPC embedded system. It is designed for easy interface to an HP 16600A/16700A-series logic analysis system. The features built into the demo board were chosen to demonstrate a variety of problems that can be solved by the logic analysis system. For ease of use, the demo board draws power from a single, logic analysis module pod or from an emulation module or probe. The demo board does not need to be configured, all features and problems are active whenever the processor is running.

In this section the following is discussed:

- how to configure the logic analysis system for use with the demo board
- what signals are mapped to the connectors
- what features are found on the demo board
- the firmware running on the demo board

Configuring the Logic Analysis System for the Demo Board

The easiest way to configure the analysis system for the demo board is to run the Setup Assistant. This is described in “Tracing Processor Code Execution with Source Code Correlation” on page 24.

For completeness, the required configuration is described here as well.

Labels and Format

The following labels and format are needed for inverse assembly. It should be noted that the demo board uses an 8 bit data bus to keep the number of analyzer pods required down to four. To use the existing 6-pod inverse assembler, some overlap is necessary between the DATA and STAT labels to make the 4-pod solution work.

Label	CLK	Pod 4	Pod 3	Pod 2	Pod 1
ADDR	----	-----	-----	*****	*****
DATA	----	*****	*****	-----	-----
STAT	****	-----*	*****	-----	-----

Clocking

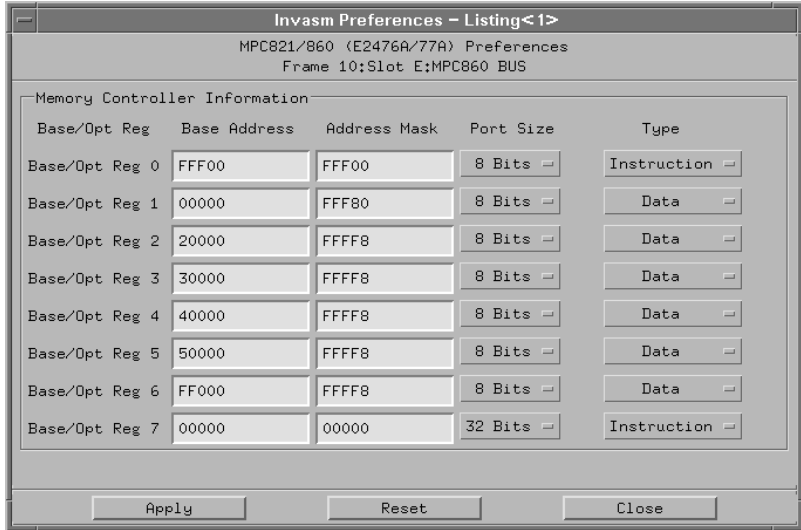
Standard inverse assembler. When using the standard inverse assembler, the state analysis clock qualifier should be set to clock on the rising edge of the J (SYSCLK) and K equal to zero (TA asserted), that is $(J^{\wedge}) * (K=0)$.

Execution trace inverse assembler. When using the cache-on execution trace inverse assembler, the state analysis clock qualifier should be set to clock on the rising edge of the J (SYSCLK), that is (J^{\wedge}) .

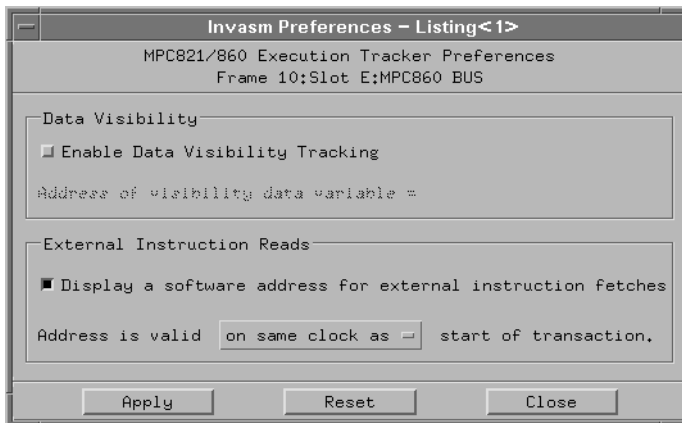
Inverse Assembler Preferences

The MPC860 processor does not provide status information as to whether it is fetching data or instructions. This information is necessary for the proper functioning of the inverse assembler. The user tells the inverse assembler where data and instructions are in the Preferences display. This display can be reached by going to the menu bar of the listing display for the MPC860 BUS analyzer. Select Invasm and then Preferences.

Standard inverse assembler. The Preference display should look like this:



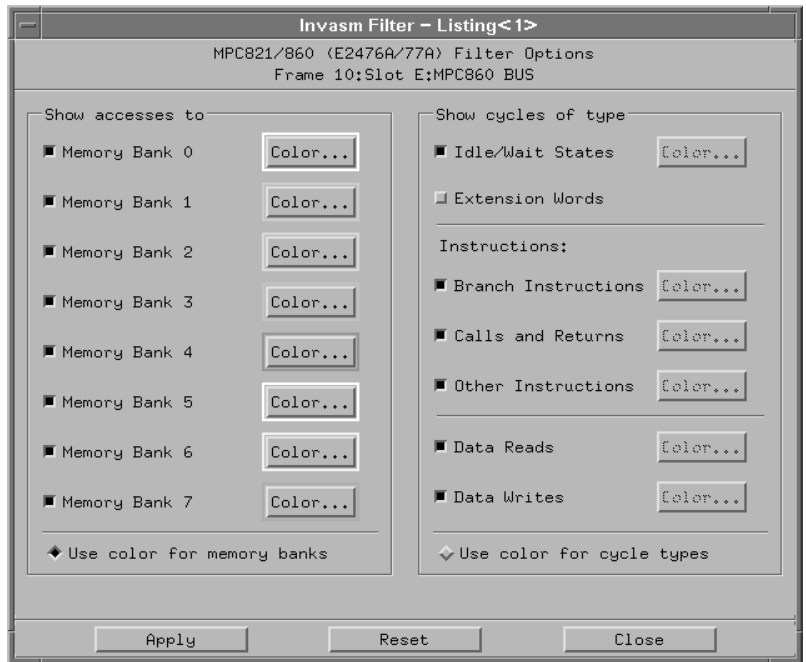
Execution trace inverse assembler. The Preference display should look like this:



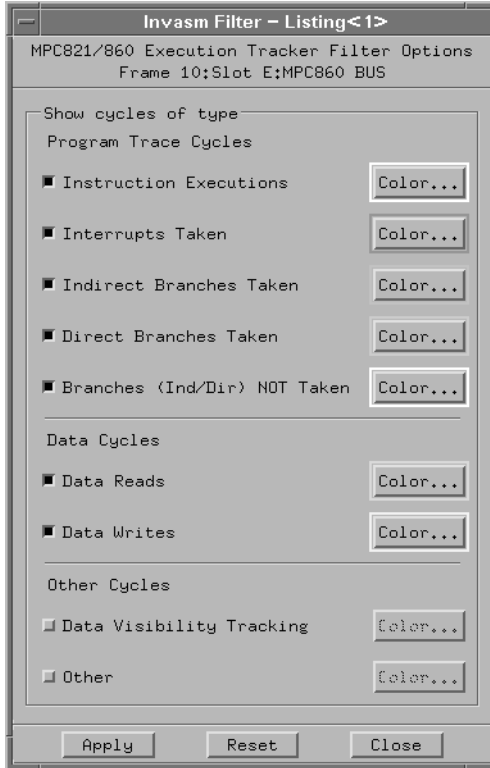
Inverse Assembler Filter

Filtering help to make the listing easier to read by suppressing some cycles and displaying others in color.

Standard inverse assembler. The demo board only has an 8 bit data bus which results in three extra bus cycles each time a data or instruction word is fetched. The filter can be set to suppress these cycles. In addition, the filter can be set to display different cycles or different areas of memory in different colors. Set the filter display to suit your tastes, the following is only an example.



Execution trace inverse assembler. The following is just an example, set the Filter display to suit your tastes:



Demo Board Connector Mapping

There are five sets of built-in connections on the demo board for connecting various system modules.

Emulation Module Connector

This connector provides a connection to either an emulation module or probe for run control of the processor. Normally this would not be a direct connection. A Target Interface Module (TIM) would be used to connect to the target's Background Debugger Mode connection or JTAG connection and then to

the emulation module. However, to eliminate the need for a TIM during demos, it has been built in.

Logic Analyzer Connectors

There are five low-density pod connections around the bottom of the demo board and six pod connections in the three Mictor38 connectors on the top of the demo board. The four listed below allow the analysis module to trace the bus cycles of the MPC860 processor.

Data	Pod 1: ADDR	Pod 2: ADDR	Pod 3: STAT	Pod 4: DATA
15	A16	A0	VFLS0	D0 - Data Bus - MSB
14	A17	A1	VFLS1	D1
13	A18	A2	AT2	D2
12	A19	A3	VF2	D3
11	A20	A4	VF0	D4
10	A21	A5	VF1	D5
9	A22	A6	$\overline{CS5}$	D6
8	A23	A7	$\overline{CS4}$	D7 - LSB (Only 8 bits used)
7	A24	A8	$\overline{CS3}$	MEM_OE
6	A25	A9	$\overline{CS2}$	MEM_WE
5	A26	A10	$\overline{CS1}$	unused
4	A27	A11	$\overline{CS0}$	unused
3	A28	A12	\overline{BURST}	unused
2	A29	A13	unused	unused
1	A30	A14	R/ \overline{W}	unused
0	A31 - LSB	A15	\overline{TS}	MODCK1
CLK	SYSCLK - 25MHz	\overline{TA}	TSIZ0	TSIZ1

Appendix A: About the MPC860 Demo Board
Demo Board Hardware

The following two pods are for timing traces of features on the demo board.

Data	Pod 5: Timing Probe	Pod 6: Pattern Generator Probe *
15	PORESET	PG15
14	HRESET	PG14
13	SRESET	PG13
12	IRQ5	PG12
11	IRQ4	PG11
10	IRQ3	PG10
9	IRQ2	PG9
8	IRQ1	PG8
7	CAN_RXD	PG7
6	CAN_TXD	PG6
5	CAN_CLK	PG5
4	DO_BOUNCE	PG4
3	unused	PG3
2	STEP_UNTERM	PG2
1	unused	PG1
0	unused	PG0
CLK	BOUNCE_LATCH	unused

* Pod 6 is only available on the Mictor38 Connector.

HP 16517A High-Speed Timing Connector

Pin	P7 - HP 16517A Connector
10 Top R	DO - Data Bus 0
9	DO_DEL - 10 ns Delayed DO
8	D1
7	D2
6	D3
5	$\overline{\text{CST}}$ - RAM Chip Select
4	$\overline{\text{MEM_WE}}$
3	$\overline{\text{MEM_OE}}$
2	$\text{R}/\overline{\text{W}}$
1 Top L	

Pattern Generator Connectors

Pin	Pattern Generator - PG1	Pattern Generator - PG2
7	LCD_DATA0 - MSB	$\overline{\text{LCD_SELECT}}$
6	LCD_DATA1	LCD_RS
5	LCD_DATA2	LCD_R/W
4	LCD_DATA3	unused
3	LCD_DATA4	unused
2	LCD_DATA5	unused
1	LCD_DATA6	unused
0	LCD_DATA7 - LSB	PG_EN

1 - PG Disabled, 0 - PG Enabled

Oscilloscope Connections

There are six scope connections on the demo board. They are used for probing various analog signals on the board. The

connections are as follows:

Label	Signal
DO BOUNCE	DO line on latch
Latch	Clock input of latch
GND BOUNCE	Ground of latch
D/A	Output of D/A converter
STEP	1 MHz signal with reflections
CAN BUS	Serial output of CAN controller

In addition, there are two ground connections for the scope probe ground clips.

Demo Board Features

Main Components

CPU.

- Motorola MPC860 Embedded PowerPC™ Microprocessor
- 25 MHz operation
- Programmed in 8-bit mode for minimal power consumption

Memory Map.

Chip Select	Device	Base Address	End Address	Size
$\overline{CS0}$	Flash ROM	0xFFF00000	0xFFFFFFFF	1 Mbytes
$\overline{CS1}$	SRAM	0x00000000	0x0007FFFF	512 Kbytes
$\overline{CS2}$	LCD	0x20000000	0x20000001	2 Bytes
$\overline{CS3}$	CAN Controller	0x30000000	0x300000FF	256 Bytes
$\overline{CS4}$	PLD	0x40000000	0x4000000F	16 Bytes
$\overline{CS5}$	D/A Converter	0x50000000	0x50000000	1 Byte
CPU	CPU Space	0xFF000000	0xFF003FFF	16K Bytes

Flash ROM.

- AMD M29F800B 1MBx8 Flash ROM
- 16 erasable sectors
- Embedded Erase/Program Algorithms
- 5 Volt Operation
- 1MB Flash ROM partitioned into protected and user blocks.

SRAM.

- Sony HM6285 512K x 8 70ns SRAM
- 512K SRAM for downloading demo code from 3rd party debuggers.

LCD.

- 2 line, 16 character display
- Optrex DMC16249

PLD.

- Altera EPM7128SQC100-15
- In-Circuit Programmable
- Contains:
 - Memory Interface
 - Interrupt Controller
 - Pattern generator interface controller
 - Hardware control registers

Features and Problems

The firmware constantly stimulates the features that need it so they are always ready for use.

Variable frequency interrupt subsystem. IRQ3 is generated by this system. It produces interrupts in varying

frequencies, with interrupts coming in a flurry, subsiding to occurring very infrequently, and then coming in a flurry again. This is intended to simulate the kind of interrupts that might occur with a LAN controller. This feature deliberately interferes with the waveform produced by the D/A converter in an asynchronous way.

LCD display with pattern generator connections. The LCD display provides feedback to the user and is driven by the processor. In addition, it is connected to the pattern generator connections through a multiplexer. When the pattern generator is connected, it can override the processor's control of the display. Vectors can be created in the pattern generator that will write to the LCD display.

NOTE:

The pattern generator by default takes control of the LCD display. When this happens, the processor will make 2,000 attempts at writing to the display before going to the following code. Needless to say, this significantly slows down the execution of the code.

Latch with a ground bounce problem. The processor writes to a latch with its ground isolated by a coil. When only a few bits change value, all is well. However, if most of the bits change value, the resulting ground bounce prevents the correct value from being written to the latch.

D/A Converter. The D/A converter is a TI TLC7528, which has 100ns settling time. The firmware stimulates the D/A converter twice each time it loops. The first time produces a triangular waveform; the second time caching is turned on and a smaller triangular waveform is produced. The triangular waveforms are distorted by IRQ2 interrupts (CAN controller) and occasionally by IRQ3 interrupts. Once in a great while the IRQ3 effect dominates the triangular waveform.

CAN Controller. The demo board includes an Intel AS82527 CAN Bus Communications Controller. The Controller Area Network (CAN) bus is primarily used by the automotive industry. This controller supports CAN 2.0 protocol. The controller provides a good example of how well the analysis

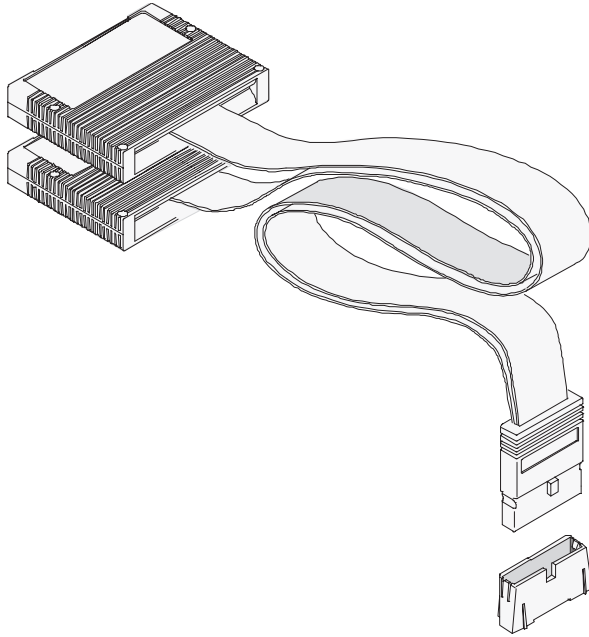
system works with external system buses. In addition, it provides an opportunity to demonstrate the serial analysis tool.

The firmware programs the controller to send out information from the Environmental Control System function each time it loops. However, CAN controllers require an acknowledge from another controller to complete a transmission. This gets simulated by the PLD, it counts the number of bytes sent by the CAN controller and then shuts it down. However, the controller is able to retransmit one more time before stopping. The IRQ2 from the CAN controller get serviced by a routine that simulates getting data from a controller that received the message.

Pushbutton. The pushbutton on the front panel labeled “Interrupt” generates an IRQ1. It can be used to generate an asynchronous event that can be detected by the analysis system.

Mictor38 probing technology. In addition to the low-density pod connections around the bottom of the demo board, there are three Mictor38 connectors on the top of the demo board. HP E5346A adapters are available to provide the connections to the analyzer pods. These connectors duplicate the low-density connections and are there primarily to demonstrate HP’s high-density connections. The footprint of these connections is reduced in two ways, the connector is smaller and no termination circuitry is required. The termination circuitry for the low-density connectors can be seen as a collection of surface mount resistors and capacitors next to the connectors.

Appendix A: About the MPC860 Demo Board
Demo Board Hardware



Demo Board Firmware

Introduction

The firmware on the 860 demo board boots the processor and initializes the board. It then prepares to execute a simulation of an Environmental Control System (ECS) and to execute code that stimulates the features and bugs built into the demo board. Then it continuously loops through the ECS and stimulus code.

Overview of main()

The function main() is located in eps2.c. It boots the processor, performs some initialization and then continuously loops through updating the display and two main functions, update_system (ECS code) and proc_specific (stimulus code). The variable num_checks is a pass counter used by update_system and update_display.

Functions and operations executed by main()

Initialization	<code>boot_q();</code> <code>init_system();</code> <code>proc_spec_init();</code>
Continuous Loop	<code>update_system(num_checks);</code> <code>num_checks++</code> <code>update_display(num_checks);</code> <code>proc_specific();</code>

What the Functions do

<code>boot_q()</code>	<ul style="list-style-type: none">• Initializes/sets up demo board (processor, PLD, etc.)• Calls <code>can_init()</code>, <code>lcd_init()</code>• Flashes LED and puts "HP Demo Board c1997" on LCD• Calls <code>pv()</code> ;Only leaves <code>pv()</code> if all is well.• Stops LED flash and puts "ECS II Ver 1. Initializing" on LCD
<code>init_system()</code>	Initializes the environmental control system. The variables are initialized within this procedure so that the system can reboot without being reloaded.
<code>proc_spec_init()</code>	Clear out the problem variable
<code>problem = 0;</code>	used to cause run-time problems CHECK ON THIS, MAY NOT BE USED
<code>main_interrupts = 0;</code>	0 - No interrupts in <code>main()</code> Set 1 for interrupts to occur in main
<code>periodic_interrupts = true;</code>	
<code>cache_on = 0;</code>	The cache is not on in <code>proc_specific</code>
<code>main_cache = 0;</code>	No effect since cache is disabled

update_system()	<p>ECS Update System Code - Modified for Demo Board. It is the service routine that alters the state of the entire environmental control system. It calls several functions, each of which have particular parts of the system that they alter or update. The following action is taken when this routine is called.</p> <ol style="list-style-type: none">1. New temperature target is read in.2. New environment conditions are read.3. The func_needed is modified based on the actual state of the environment versus the desired state to indicate what needs to happen in the current environment.4. func_needed is used to derive hwr_encode (the 16-bit quantity that indicates what the hardware needs to do to achieve the correct change in the environment).5. The environment conditions are saved for posterity.6. THERE IS A BUG IN THIS ROUTINE (ON PURPOSE!!!)
update_display()	<p>Clear out the history buffer and update the current ascii display of operating data (ascii_old_data).</p>
proc_specific()	<p>Proc_specific exercises all of the features and bugs built into the demo board. There is a detailed description of what proc_specific does below.</p>

Where the functions are located

Function	Location
main()	ecs2.c
boot_q	boot.c
can_init	can.c
init_system	init_sys.c
lcd_init	lcd.c
proc_spec_init	proc_spec.c
proc_specific	proc_spec.c
pv	pv.c
update_display	ecs2.c
update_system	update_sys.c

Overview of proc_specific

Turn on the cache if `cache_on = 1`

Start up the periodic interrupts

Display ECS status on the LCD

Stimulate the Controller Area Network (CAN) Bus

The following data will be sent out the CAN bus. Each variable is 8-bits, with an 8-bit label that precedes it in the data transmission. With the serial analyzer, look for the 0x11, 0xaa, 0x22, 0xbb, etc. to know which variable's data follows.

Stimulate the D/A Converter

The D/A converters output voltage is 5 volts times $D/256$. Create a triangle wave by ramping up the voltage one step at a time, then immediately ramping it down.

Stimulate the ground bounce register

The demo board has register with a ground bounce problem. Connect the scope to the 'D0 Bounce' and 'Latch' Signals.

Trigger the scope on the rising edge of 'latch' with a threshold of 1.5 volts and a sample rate of at most 5ns. Note the change in 'D0 Bounce' when data line changes.

Run a piece of code in cache

The following instruction can be used to trigger on if running the MPC860 execution tracker software on the logic analyzer. Note that even if indirect only show cycles are on, the logic analyzer can trigger.

Note that this section will be skipped if the cache is already on.

Return to normal ECS code

Before returning, check if any of the execution flags have been set - if `main_interrupts = 0`, Turn off interrupt activity before leaving function. If `main_cache = 0`, Turn off the cache for main.

Variables

Variables of interest

The following are some of the key variables in the demo board firmware.

Variable	Remarks	See Also
<code>ascii_old_data</code>	ASCII values of temperature data. It is used to show the value of a debugger to monitor complex C variables. Historically, 'printf' was used to write various values to a port on a regular basis. This is inherently slow and may require the use of a dedicated port on the target. A better alternative is to use 'sprintf' to write to RAM and display that memory using a debugger. While 'sprintf' incurs the same overhead as 'printf' for data conversion, there is no interaction with the outside world required.	<code>update_display</code>
<code>cache_on</code>	0 - (default) The cache is off 1 - The cache is on in <code>proc_spec()</code>	<code>main_cache</code>
<code>curr_loc</code>	Location to write old temp, incremented past end of <code>old_data</code>	<code>old_data</code>

Appendix A: About the MPC860 Demo Board Demo Board Firmware

Variable	Remarks	See Also
current_temp	Current temperature, used by ECS program.	
func_needed	It is the byte that indicates what the ECS code needs to do to the environment. The following specifies the values it may have: <pre> bit bit #1 bit #0 function needed cool heat </pre> The only valid values for this char are: (hex) (binary) (1) 0001 heat (2) 0010 cool	
hdwr_encode	It is the encoded 16-bit quantity output by the system which is interpreted by external devices. It tells the external devices what to do, for example, turning the air conditioner on (indicated by hdwr_encode = 0010). There are four sets of four bits within the 16 bit quantity hdwr_encode. These sets of bits are encoded as follows: <pre> bits 7 - 4 bits 3 - 0 Air Conditioner Heater 0 = off 0 = off 1 = on 1 = on </pre>	
main_cache	0 - (default) The cache is on in proc_spec() (only checked if cache_on = 1) 1 - The cache is on in all modules	cache_on
main_interrupts	0 - (default) No interrupts in main() 1 - Interrupts in main()	
MaKeBaR	MaKeBaR Set to zero to turn off all MAKEBAR's in ECS code, which speeds up the code.	
num_checks	Counts the number of times update_system() is called	
old_data	History of temp data, used by ECS code. Code writes past the end of old_data into target_temp, creating a bug.	curr_loc
outside_temp	Outside temperature, used by ECS code	
target_temp	Target temperature, used by ECS code	
temp_target	Used by ECS code to ramp target_temp; specifies limits	

Markers, special variables

The following variables are used to instrument the code. They come in ME_ and MX_ pairs. The ME_ variable is used to mark

when a function is entered by writing a one to it as the first instruction in the function. The end of the function is marked in the same way except a one is written to the MX_ variable when exiting the function. The analyzer can be set up to trace just the addresses at which a write to the variable pairs occurs, thereby tracing the beginning and end of the functions instrumented. The analyzer can keep track of the time between the writes and there can come up with a trace of how long the software spends in each function over a long period of time.

The ME_first_marker and MX_last_marker are used to make it easy to set a range across all the code without having to know the exact addresses.

```
ME_first_marker
ME_update_system
MX_update_system
ME_update_display
MX_update_display
ME_clear_hist_buff
MX_clear_hist_buff
ME_proc_specific
MX_proc_specific
ME_do_sort
MX_do_sort
ME_get_targets
MX_get_targets
ME_read_conditions
MX_read_conditions
ME_set_outputs
MX_set_outputs
ME_write_hdwr
MX_write_hdwr
ME_save_points
MX_save_points
ME_add_to_history
MX_add_to_history
MX_last_marker
```

Using the PowerPC 860 Emulation Module

Do not run from reset. Break from reset; then, run. Otherwise, the default DER register setup will not allow setting hardware breakpoints. The copy from the emulation module's CF_DER register doesn't occur.

Recommended Demo Configuration

Why use Recommended Demo Configuration

All of the exercises in this guide, except for the ones in the “Quickly Set Up the Analysis System” chapter on page 15, rely on loading configuration files that were developed on an analysis system with a particular configuration. If the files are loaded into a system that has a different configuration of modules, the exercises may or may not work. This is because different analysis modules have different trace depths and different internal configurations. The analysis system will attempt to load the configuration files in the best way possible, which will allow some of the configuration to work.

Two of the exercises, “Using the pattern generator” on page 111 and “Using the high-speed logic analyzers” on page 121, only use a single module. These exercises should work no matter which slot their respective modules are in.

What is the Recommended Demo Configuration

The recommended demo configuration is as follows:

Analysis System Slot	Module	Required for:
A	HP 16517A	1 exercise
B	HP 16522A	2 exercises
C	HP 16534A	most exercises
D	HP 16555D, extension	most exercises
E (bottom)	HP 16555D, master	most exercises

Most exercises also require an HP 16610A emulation module, preferably in slot 1.

Module Descriptions.

HP16555D - 2M Sample, 110 MHz State/500 MHz Timing

Appendix A: About the MPC860 Demo Board Recommended Demo Configuration

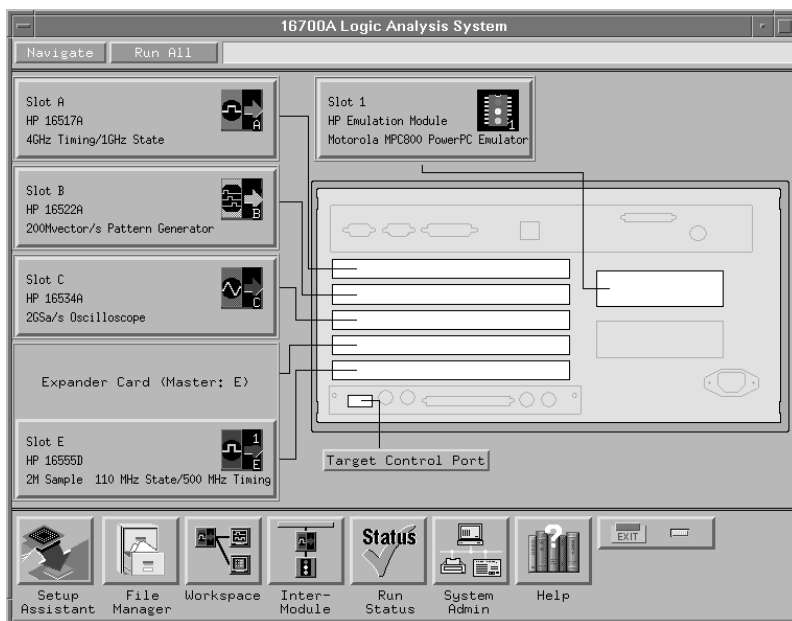
HP16534A - 2 GSa/s, 2 Ch. Oscilloscope

HP16522A - 200Mvector/s, 40 Ch. Pattern Generator

HP16517A - 4 GSa/s Timing/1 GSa/s State, 16 Channel

Verifying Your Configuration

Start an analysis session and look at the HP 16700 system window. Look at the analysis module buttons down the left side of the window. They should be as follows:



B

Concepts

Timing Analysis vs. State Analysis in Logic Analyzers

Timing analysis with a logic analyzer is much like tracing a signal with a digital oscilloscope. A scope samples the signal at a rate established by an internal clock and displays it on a screen for viewing. A logic analyzer differs from a digital scope in that one-bit comparators rather than eight-bit are used. This establishes two signal levels (logic 1 or 0) rather than the continuous range of signal levels that you get with a scope. As a result, logic analyzer channels are much cheaper than a scope's, allowing many more to be put in a single instrument.

With a large number of channels, the logic analyzer can show the timing relationship of logic between various signals in a large variety of systems. For example you could look at the timing relationship between the logic levels of the control lines, address lines, and data lines of a processor. However, you may be more interested in a sequence of states on the processor's bus than the timing relationship of the bus elements. This acquisition would be best if each state were acquired only when they were valid. In other words, synchronous with the bus clock.

When you want to capture signals that are synchronous with clocks or other signals in the target system, the logic analyzer can use external clock signals for sampling data. Of course, the clock edge you give to the logic analyzer must sample target system data when it is valid. When an external clock is being used for sampling, the logic analyzer is configured as a *state analyzer*.

Glossary

A

analysis probe A special type of probe for connecting the logic analyzer to microprocessors or standard busses. Analysis probes typically include files for configuring the logic analyzer and labeling channels, as well as inverse assemblers for decoding captured bus cycles into assembly language instructions.

arm A condition that enables an instrument and allows it to trigger. You can set up one instrument to arm another using the Intermodule window. In some analyzer instruments, you can set up one analyzer machine to arm the other analyzer machine in the Setup window's Trigger tab.

C

channel A single probe for capturing data on one signal.

clock inputs (labeled J, K, L, M, etc.) The clock inputs on the logic analyzer pods are labeled J, K, L, M, etc. for pods 1, 2, 3, 4, etc., respectively. We have preserved this labeling to maintain continuity with previous logic analyzers.

E

emulation adapter Attaches to an emulation module and has a special connector for interfacing with a microprocessor's debug port connector.

emulation module A module that can be installed in the HP 16700A-series logic analysis system to provide the ability to run, step, or stop microprocessor execution, set breakpoints, and modify the contents of microprocessor registers and memory locations.

emulation probe A stand-alone emulation module and adapter combination that can exist on the Local Area Network (LAN) and be used with 3rd-party debuggers or the HP 16700A-series logic analysis system.

L

logic analyzer An instrument that captures digital signals.

labels Names given to logic analyzer channels. Typically, these names correspond to the signals or busses they are probing.

Glossary

M

machine A collection of logic analyzer channels that can be configured independently as a timing analyzer or as a state analyzer.

module An instrument that uses a single time base in its operation. Modules can have from one to five cards functioning as a single instrument. When a module has more than one card, they main system window will show the instrument icon in the slot of the master card.

O

oscilloscope An instrument that captures analog signals and the analog parameters of digital signals.

P

pod A group of logic analyzer channels. These are the 2x20 connectors on the end of the cables coming out of the logic analyzer. A pod is assigned to a virtual analyzer by dragging it to the area below the analyzer's name.

pod pair All current HP logic analyzer modules group their pods into pod pairs.

processor solution A bundled HP product that includes an analysis probe, and emulation module, and the source correlation tool set.

S

sequencer A state machine in the logic analyzer's data recognition and filtering circuitry that is used to identify when data should be captured (in other words, when the logic analyzer should trigger).

state analysis When data is sampled at a rate determined by clocks external to the logic analyzer.

T

target system The system under development whose digital signals you are measuring.

timing analysis When data is sampled at a rate determined by the logic analyzer's internal clock.

Glossary

trigger The reference point in a logic analyzer measurement.

tool set An add-on software product for the HP 16700A-series logic analysis system.

V

virtual analyzer Virtual analyzers provide a way of grouping the different signals you collect. For the most part, you won't have to worry about having two virtual analyzers, just group all your active pods under one analyzer and proceed to the format tab of the setup dialog. However, there are times when you must use two analyzers, such as when you want to collect both state and timing traces.

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